A Single- and Three-Phase Grid Compatible Converter for Electric Vehicle (EV) On-Board Chargers

Hui Zhao, *Member, IEEE*, Yanfeng Shen, *Member, IEEE*, Wucheng Ying, Saikat Subhra Ghosh, *Student Member, IEEE*, Md Rishad Ahmed, *Member, IEEE*, and Teng Long, *Member, IEEE*

***Abstract*- This paper proposes a voltage-source converter for an on-board Electric Vehicle (EV) charger which is compatible with both the single- and three-phase (1-ϕ and 3-ϕ) grids. The classic 3-ϕ active AC-DC rectifier circuit is used for both the 1-ϕ and 3-ϕ connection, but a new control scheme and *LCL* filter are designed to address the double-line frequency power pulsation issue caused by a 1-ϕ grid without using bulky DC capacitors. The third leg of the circuit is utilized to control the power pulsation in conjunction with stored energy in the *LCL* filter between the grid and charger rectifier. Neither additional active nor passive components are required. For the 3-ϕ connection, the rectifier is under balanced operation; when connected with the 1- ϕ grid, all three legs are controlled cooperatively as a 3-ϕ rectifier but under unbalanced operation to recreate the 1-ϕ voltage. Hence advantages from the 3-ϕ rectifier such as space vector pulse width modulation (SVPWM) and Y/Δ transformation can be utilized to increase utilization of DC-link voltage and filter capacitance respectively. The operation principle, control, and *LCL* filter design are reported and validated by both simulation and experiments of a 3-kW porotype.**

***Index Terms*- 1-ϕ and 3- ϕ compatible rectifier, EV battery on-board charger, double-line frequency power pulsation, power decoupling.[1]**

I. Introduction

The on-board charger (OBC) for Electric vehicles (EVs) is attracting increasing attention [1-4] because of a rapid uptake of transport electrification [5, 6]. Major automobile production and consumption countries such as the U.S. and the U.K. have set ambitious EV development roadmaps in which the OBC has been defined as an important aspect [7, 8]. By 2035, the gravimetric and volumetric power densities of the OBC are expected to achieve 50 kW/kg and 60 kW/L according to the roadmap, which are approximately seven times higher than existing products [8].

The Level 2 charging in which an AC supply with the current up to 60 A is fed has been commonly considered as a mandatory requirement for OBCs in the domestic and street-side charging [9, 10]. The voltage of such AC supplies can be either single-phase (1-ϕ) or three-phase (3-ϕ). In fact, without additional upgrade on circuit breakers, 3-ϕ supplies can effectively increase the charging rate by three times, showing a sensible and affordable solution for EV charging. The 3-ϕ supply is commonly available in premises and thus it is commercially valuable to equip the EV OBCs with both 1-ϕ and 3-ϕ grid connections [11, 12]. Yet most of commercial OBCs are only compatible with a 1-ϕ supply and it is hardly seen literature on combined 1-ϕ and 3-ϕ OBCs. The potentials of such technology and solution have been overlooked by both the industry and academia.

However, the difference and challenge of combining single- and 3-ϕ OBCs are beyond only adding one more leg in the AC-DC rectifier of the OBC. When the OBC is connected to a 1-ϕ supply, a large power pulsation at double line frequency [13] is generated at the AC-DC rectifier, which would not appear when connecting to a 3-ϕ supply. In this paper, the AC-DC rectifier of the OBC as shown in Fig. 1 is focused to enable both single- and 3-ϕ OBC connection and achieve high power density.

TABLE I summarizes the techniques dealing with this double-line frequency power pulsation. Conventional techniques usually employ a bulk DC capacitor bank to reduce the voltage pulsation at the DC link of the rectifier. The power density is low due to the large number of capacitors at the DC-

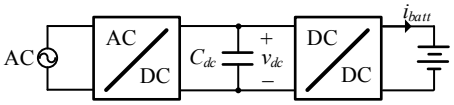
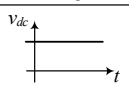
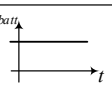
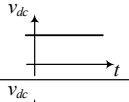
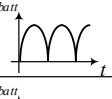
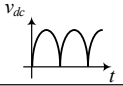
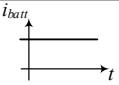
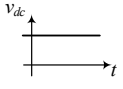
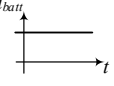


Fig. 1. The diagram for EV chargers with a 1-ϕ grid.

TABLE I
Comparison among different Techniques to Resolve the Double-Line Frequency Power Pulsation

Method	DC link voltage	Charging current	Main issues
DC capacitor storage			Large DC capacitor
Fluctuate charging current			Impairing battery
Variable DC voltage			High voltage stress; Over modulation
Active power filter (APF)			Extra switching devices for control; Extra passive devices for energy storage

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H. Zhao, Y. Shen, W. Ying, S. S. Ghosh and T. Long are with the Department of Engineering, University of Cambridge, Cambridge CB3 0FA, U.K. (e-mail: hz352@cam.ac.uk; ys523@cam.ac.uk; wy256@cam.ac.uk, ssg39@cam.ac.uk, tl322@cam.ac.uk).

M. R. Ahmed is with the Dynex Semiconductor, Lincoln LN6 3LF, U.K. (email: rishadahmed@yahoo.com).

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link. The reliability is also limited because the use of less reliable electrolytic capacitors is usually inevitable in this technique to achieve large capacitance.

To increase the power density, [14] boldly directs the low frequency power pulsation into the batteries so the capacitance of the DC-link can be significantly reduced but the DC current provided by the OBC contains a large AC ripple at the double-line frequency although the impact of the low frequency ripple current at to the batter is unclear. Some literature [15, 16] shows that the current pulsation will cause an adverse impact on the battery[17] such as the temperature increase, the capacity degradation, and the gassing.

Advanced control techniques can eliminate the current distortion caused by the double-line frequency power pulsation. [18] employs a repetitive algorithm and a feed-forward controller to eliminate the output current distortion. [19] applies a feedback controller to reduce the current pulsation. However, those special control techniques are based on using the inconstant DC-link voltage largely pulsating at the double-line frequency to smooth the output DC current and a high control bandwidth must be employed. The pulsating DC voltage will cause voltage stress and over-modulation of semiconductors at the peak and bottom of the pulsation respectively.

The active power filter (APF) can divert and store the double-line frequency power pulsation by using much smaller energy storage components. There are different APF circuit topologies depending on the location of the APF and the type of components used for energy storage in the APF [13, 19-30]. The APF can be implemented at the DC side [24, 25, 27] as shown in Fig. 2 (a) or AC side as shown in Fig. 2 (b) [13, 29, 31]; there are inductor-based APFs [24] and capacitor-based APFs [13, 20, 21, 27]. To identify the optimal location and the type of the energy storage components used in APFs, the unified equations among these techniques are necessary.

Reducing the cost and size of the APFs are important. [20] uses split-capacitors to control the current in both the rectifier and APF, and thus no extra switches are required. However, extra passive components are still needed to store the pulsating power. [30, 32] use novel topologies to reduce the capacitance but the voltage ratings of the capacitors and the semiconductor devices must be increased. Since the passive components storing the pulsating energy can dominate the volume and weight of the APF, it is important to investigate the volume/weight of the energy storage components.

This paper proposes a universal converter which is compatible with both a 1-ϕ and 3-ϕ supplies. Unlike some other chargers [11, 12] in which the third leg of the rectifier is redundant when connected to a 1-ϕ supply, the proposed technique utilizes the third leg as part of the AC side APF to address the double-line frequency power pulsation issue while the other two legs are connected to the 1-ϕ AC supply. Furthermore, the low frequency power pulsation is diverted into the *LCL* filter between grid and converter and the capacitor at the *LCL* filter is used to store the power pulsation. Therefore, neither extra semiconductor nor passive components are required. From control's perspective, unlike the conventional APF technique, which decouples and separately controls the dc

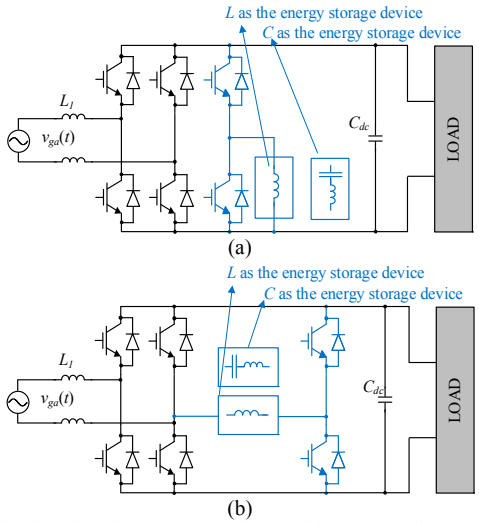

Fig. 2. The circuits of typical APFs: (a) the DC side APF, (b) the AC side APF.

power and the double-line frequency power pulsation, the proposed control operates three legs as an unbalanced converter when connected with a 1-ϕ supply. Therefore, some benefits from 3-ϕ converters can be utilized, namely, the Y/Δ transformation and space vector pulse width modulation (SVPWM) can be applied to amplify the equivalent capacitance in *LCL* filters for APF power pulsation storage and achieve higher DC voltage utilization compared with sinusoidal pulse width modulation (SPWM), respectively. When connected with a 3-ϕ supply, the third leg is used with the other two legs like a normal 3-ϕ rectifier and no APF is needed because no double-line frequency power pulsation exists.

The paper is organized as follows: section II derives the universal equations to evaluate the optimal APF circuit. Section III proposes the circuit and discusses its operation principle. Section IV discusses the parameter design procedure of the *LCL* filter for this combined single- and 3-ϕ rectifiers along with the size and weight comparison with the conventional circuit. Section V presents simulations and experiments to verify the design.

II. Evaluations of Double Line Frequency APFs Based on Unified Equations

Various APFs exist to filter the double line frequency power pulsation of a 1-ϕ rectifier. Fig. 2 (a) and (b) show the APF at the DC side AC side respectively. Either the inductor *L* or capacitor *C* or both can be used at the AC and DC side as energy storage components. Because both the topology and type of energy storage components can affect the current / voltage waveforms so does the power density of the APF, identifying the optimal circuit is complicated. A unified expression is derived to assess the performance of the different type of APFs as well as the volume expressions for the passive components are defined to support the selection of the APF in order to minimize the size of the passive components.

A. Evaluating the Size and Weight of Inductors and Capacitors as Energy Storage Devices for APFs

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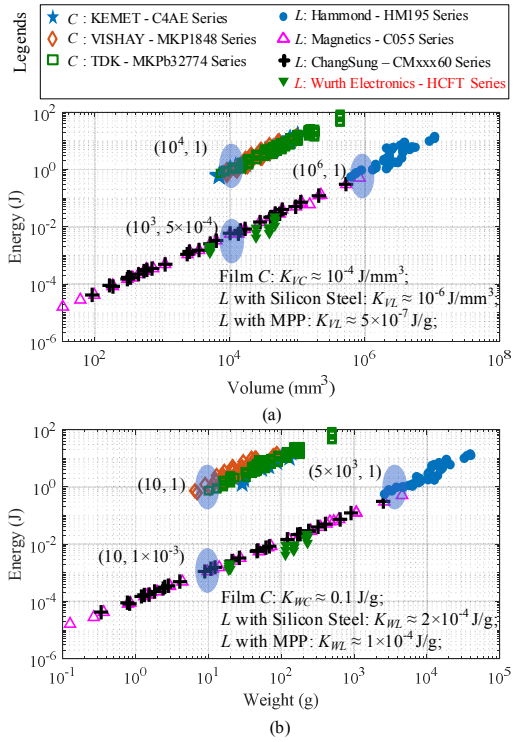

Fig. 3. The relationship between the volume/weight and the maximum energy storage for the inductors and film capacitors: (a) the energy vs the volume, and (b) the energy vs the weight.

To discuss the relationship between the volume/weight versus the maximum stored energy, Fig. 3 (a) and (b) records 241 different capacitors and 121 different inductors from the market, including 49 inductors with silicon steel cores from the Hammond Manufacturing [33], 36 inductors with MPP power cores from the Magnetics Inc[34], 36 inductors with MPP power cores from ChangSung Corp [35], 19 inductor from Wurth Electronics's HCFT series, 53 film capacitors from KEMET [36], 49 film capacitors from Vishay [37], and 139 film capacitors from TDK [38]. It should be noted that the weight information of 39 capacitors from C4AE series is not available in the datasheets so the *Energy* v.s *Weight* relationship shown in Fig. 3 (b) contains 199 capacitors while Fig. 3 (a) contains all 238 capacitors to illustrate the *Energy* v.s *Volume* relationship. Moreover, to calculate the size and volume of inductors with MPP cores, the maximum magnetic flux density is set as 0.1 T and the fill factor = 0.4 is used as a typical value suggested in Magnetics Inc's design guides [39] in toroidal cores. The commercial inductors have two current limits: the saturation current (donated by I_{sat}), the current for temperature rise (donated by I_{rms}). When evaluating the maximum energy storage capability, the rated current (donated by I_{rated}) is employed, which is the minimum value of I_{sat} and I_{rms}, so that both the saturation constraints and the temperature constraints, are considered in Fig. 3.

Fig. 3 shows that, although the size/weight difference with different manufacturers/series, the volume/weight of both the inductors and capacitors are approximately linear with their maximum energy storage. This linear relation can be expressed as (1) and (2) for inductors and capacitors:

$$\begin{cases} Eng_L = \frac{1}{2} L I_{rated}^{\ 2} = K_{VL} \bullet VOL_L \\ Eng_L = \frac{1}{2} L I_{rated}^{\ 2} = K_{WL} \bullet WET_L \end{cases} \quad (1)$$

$$\begin{cases} Eng_C = \frac{1}{2} C V_{rated}^{\ 2} = K_{VC} \bullet VOL_C \\ Eng_C = \frac{1}{2} C V_{rated}^{\ 2} = K_{WC} \bullet WET_C \end{cases} \quad (2)$$

where Eng_L / Eng_C is the maximum energy which can be stored in the L / C; I_{rated} / V_{rated} is the rated maximum current/voltage, VOL_L / WET_L, and VOL_C / WET_C are the volume/weight of the inductor and capacitors, K_{VL} / K_{WL} and K_{VC} / K_{WC} the energy density coefficients per unit volume/weight for inductors and capacitors.

Large energy density coefficients can result in small volume/weight. In Fig. 3, all the energy density coefficients can be obtained by choosing a specific point (as highlighted with blue in Fig. 3). For film capacitors, $K_{VC} \approx 10^{-4}$ J/mm^3, and $K_{WC} \approx 0.1$ J/g; for silicon steel inductors, $K_{VL} \approx 10^{-6}$ J/mm^3, and $K_{WL} \approx 2\times10^{-4}$ J/g; for inductors with MPP cores, $K_{VL} \approx 5\times10^{-7}$ J/mm^3, and $K_{WL} \approx 1\times10^{-4}$ J/g.

B. Unified Voltage and Current Equations of APF at the DC and AC Sides

To derive the equation, an inductor is used for storing energy at the DC side APF as shown in Fig. 2 (a). The double-line frequency (notated as subscript 100 as the line frequency is considered as 50 Hz) power pulsation $p_{100}(t) = P_{100}\sin(2\omega_g t+\theta)$ needs to satisfy:

$$v_l(t) i_l(t) = L \frac{di_l(t)}{dt} i_l(t) = P_{100} \sin\left(2\omega_g t + \theta\right) \quad (3)$$

where the $i_l(t)$ and $v_l(t)$ are the inductor current and voltage respectively; L is the inductor; ω_g and θ are the grid's angular frequency and phase angle respectively, $p_{100}(t)$ is the double line frequency power pulsation, and P_{100} is its magnitude.

The solution of (3) is (4),

$$\begin{cases} i_l(t) = \pm\sqrt{\frac{P_{100}}{\omega_g L}}\sqrt{\left(K - \cos\left(2\omega_g t + \theta\right)\right)} \\ v_l(t) = \pm\sqrt{P_{100}\omega_g L}\frac{\sin\left(2\omega_g t + \theta\right)}{\sqrt{\left(K - \cos\left(2\omega_g t + \theta\right)\right)}} \end{cases} \quad (4)$$

where K is the constant in general solutions of the differential equations, determined by $i_l(0)$ as: $K = i_l(0)\frac{\omega_g L}{P_{100}} + \cos(\theta)$. Because $i_l(0)$ can be controlled by setting specific value, K is determined by the control strategy. $i_l(t)$ must be a real number so $K \geq 1$ is required. Specially, when $K = 1$, (4) can be further simplified as,

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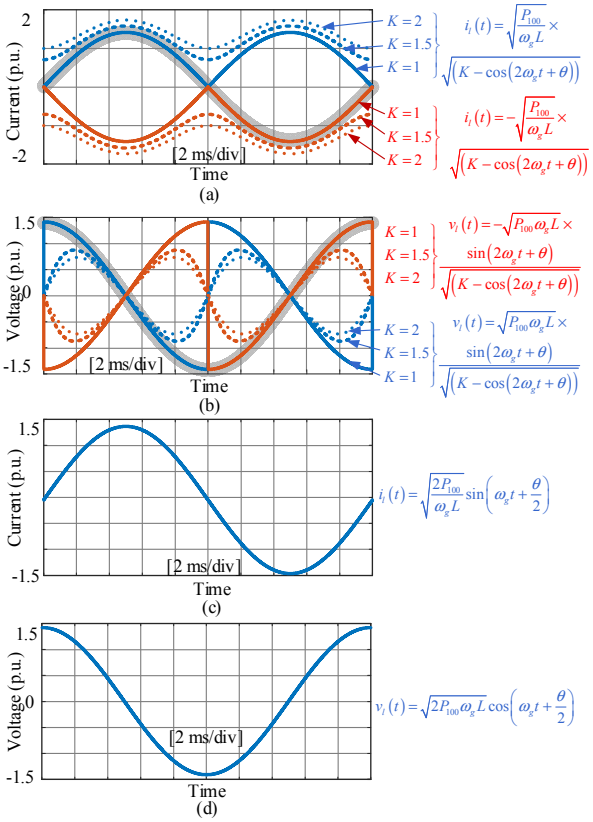

Fig. 4. The waveforms for inductors as energy storage components: (a) $i_l(t)$ in the DC side APF, (b) $v_l(t)$ in the DC side APF, (c) $i_l(t)$ in the AC side APF, and (d) $v_l(t)$ in the AC side APF.

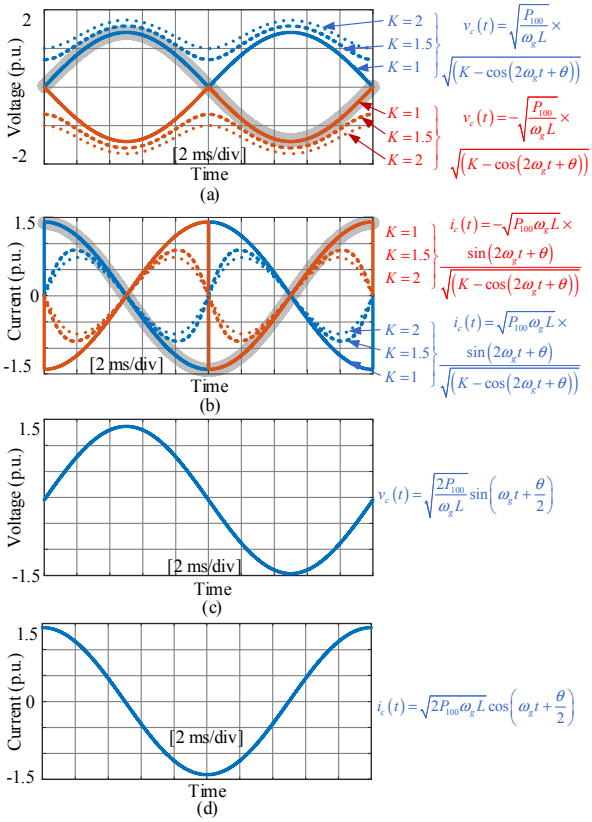

Fig. 5. The waveforms for capacitors as energy storage components: (a) $i_l(t)$ in the DC side APF, (b) $v_l(t)$ in the DC side APF, (c) $i_l(t)$ in the AC side APF, and (d) $v_l(t)$ in the AC side APF.

$$\begin{cases} i_l(t) = \pm\sqrt{\dfrac{2P_{100}}{\omega_g L}}\sin\left(\omega_g t + \dfrac{\theta}{2}\right) \\ v_l(t) = \pm\sqrt{2P_{100}\omega_g L}\cos\left(\omega_g t + \dfrac{\theta}{2}\right) \end{cases} \tag{5}$$

Fig. 4(a) and (b) show the waveforms of $i_l(t)$ and $v_l(t)$ at different K for the DC side APF. When $K \geq 1$, the DC offset of the inductor current occurs and both the mean and peak values increase when K increases. As shown in Fig. 4(a)-(b), the blue/red curves represent the positive/negative solutions in (4). When $K = 1$, the shape of the $i_l(t)$ is sinusoidal within both [0, 10] ms and [10, 20] ms as the grey curves, but $i_l(t)$ flips over at the communication point when $t = 10$ ms so its polarity remains unchanged. This flip-over of $i_l(t)$ will flip $v_l(t)$ because $v_l(t) = Ld i_l(t)/dt$.

If L is installed at the AC side, the equation to compensate P_{100} is as same as (3) and the solution remains as same as (4). However, the value K can only be 1 because the $i_l(t)$ of the AC side APF needs a natural commutation point to change the polarity and there is no DC offset. Therefore, $K = 1$ is mandatory. $i_l(t)$ and $v_l(t)$ are shown in Fig. 4 (c) and (d). From existing literature, (4) has been verified by both DC side APFs in [27, 40] and AC side APFs in [13].

C. Volume/Weight Expressions of Passive Components

Based on the unified solution in (4), the magnitude of $i_l(t)$ for AC side APF and DC side APF has the same expression as shown in (6).

$$mag\left(i_l(t)\right) = \sqrt{P_{100}\Big/\left(\omega_g L\right)}\sqrt{(K+1)} \tag{6}$$

From (6), it is obvious that the AC side inductor current equals to the smallest value of that in the DC side APF for storing the same amount of energy, i.e. $K = 1$. The inductance L and inductor current $i_l(t)$ determine the volume of inductors.

Substituting (6) into (1) yields (7):

$$\begin{cases} VOL_L = \left(\dfrac{1}{2}LI_{rated}{}^2\right)\Big/K_{VL} = \dfrac{P_{100}}{2\omega_g K_{VL}}(K+1) \\ WET_L = \left(\dfrac{1}{2}LI_{rated}{}^2\right)\Big/K_{WL} = \dfrac{P_{100}}{2\omega_g K_{WL}}(K+1) \end{cases} \tag{7}$$

Eq. (7) shows that the volume/weight of the required inductance is determined by the power pulsation (P_{100}), the material (K_{VL} / K_{WL}), and the control stratagem (i.e. the value of K) from (6).

When a capacitor is applied as the energy storage device, similar to the derivation of using the inductor, the double-line power pulsation needs to satisfy (8), where v_c and i_c are the voltage and current of the capacitor used in APF respectively. The general solutions of (8) are given in (9) and the volume expressions are in (10). As aforementioned, the solution and

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volume expressions of capacitor based APF in (8) and (9) are applicable for both the AC and DC side APFs. For DC side APF, $K \geq 1$. For AC side APF, $K = 1$. The voltage and current waveforms of the capacitor at the DC and AC side APF are shown in Fig. 5.

$$v_c(t)i_c(t) = v_c(t)C\frac{dv_c(t)}{dt} = P_{100}\sin\left(2\omega_g t + \theta\right) \tag{8}$$

$$\begin{cases} v_c(t) = \pm\sqrt{\dfrac{P_{100}}{\omega_g C}}\sqrt{K - \cos\left(2\omega_g t + \theta\right)} \\ i_c(t) = \pm\sqrt{\dfrac{P_{100}}{\omega_g C}}\dfrac{\sin\left(2\omega_g t + \theta\right)}{\sqrt{\left(K - \cos\left(2\omega_g t + \theta\right)\right)}} \end{cases} \tag{9}$$

$$\begin{cases} mag\left(v_c(t)\right) = \sqrt{\dfrac{P_{100}}{\omega_g C}}\sqrt{K+1} \\ VOL_C = \left(\dfrac{1}{2}CV_{rated}{}^2\right)\Big/K_{VC} = \dfrac{P_{100}}{2\omega_g K_{VC}}(K+1) \\ WET_C = \left(\dfrac{1}{2}CV_{rated}{}^2\right)\Big/K_{WC} = \dfrac{P_{100}}{2\omega_g K_{WC}}(K+1) \end{cases} \tag{10}$$

where VOL_C / WET_C is the volume/weight of the capacitor, and K_{VC} / K_{WC} is the energy density per unit volume/weight.

Because (10) has the same form to (7), one unified equation can be used to assess the volume and weight of the APF passive components, which depends on the location of the APF in terms of the value K and the type of the passive components in terms of the value of K_L and K_C.

D. Optimal Circuit Selection

From Fig. 5, it is obvious that the capacitor shows higher energy density than inductors considering both the size and weight, i.e. $K_{VC} \gg K_{VL}$ and $K_{WC} \gg K_{WL}$, so the APF is in favour of using film capacitors for storing energy. However, as shown in Fig. 2, the voltage source APF with a capacitor needs an extra inductor for ripple current damping and limiting, which needs to be considered in the design.

Existing techniques [25, 30, 41] use capacitance per watt (F/W) to identify the optimal circuit, and propose the APFs with small capacitance but a high voltage rating. However, the volume/weight of capacitors in different types of APFs have not been compared. The unified volume expression in (10) can be used to identify the circuit with optimal volume and weight.

In (10), P_{100}, ω_g. K_M are constant, and the only controllable parameter is K. To achieve the minimum volume, $K = 1$ should be selected no matter AC side or DC side APFs. However, when $K = 1$ of the DC side APF, the control variables, capacitor current and voltage $i_c(t)$ and $v_c(t)$, are non-sinusoidal with sharp changes as shown in Fig. 4 and Fig. 5. The widely spread spectrums of the voltage and current require a high control bandwidth to be implemented at the APF and the filtering performance is inevitably compromised [27]. Furthermore, the parasitic components might dominate the high-frequency impedance, resulting in errors of the instantaneous power equation in (3).

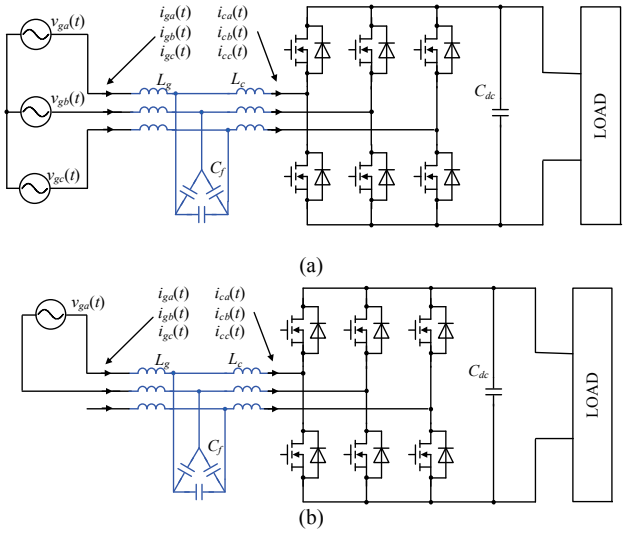

Fig. 6. The proposed universal converter operates (a) with a 3-ϕ grid, and (b) with a 1-ϕ grid.

Instead, K must be 1 when the AC side APF and both the voltage and current are sinusoidal. The control of side APF is much easier than the DC counterpart for the same power density of the APF so the filtering performance of the APF at the AC side is better.

In conclusion, the APF using capacitors at the AC side has the advantages of low volume, low bandwidth control requirements, high filtering performance and robustness with parasitic parameters thus it has been selected in this paper.

III. Proposed Universal 1-Φ and 3-Φ Topology and Control for AC-DC Rectifier Used in OBCs

The proposed universal 1-ϕ and the 3-ϕ circuit is as shown in Fig. 6. When connected with a 1-ϕ supply, the third leg of the rectifier can be utilized to control the power flow to compensate the double-line frequency power pulsation, therefore no extra power electronic switches are required for the APF functionality. Moreover, the *LCL* filter between the supply and the converter can be utilized as energy storage components thus no extra passive components are required. Because the *LCL* filter inherently has inductors, no additional ripple current damping inductors are required in the APF.

The *LCL* filter in Fig. 6 is highlighted in blue to emphases that it not only attenuates the switching harmonics but also stores the unbalanced power pulsation when used as part of the APF for a 1-ϕ connection.

A. Double-Line Frequency Power Pulsation in Form of Sequence Networks

The instantaneous power $p(t)$ can be written in the form of sequence network, where the subscripts 0, 1, 2 donate the zero sequence, positive sequence, and negative sequence respectively. If no zero-sequence current exists, the expression of $p(t)$ is shown as (11):

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TABLE II
THE DC POWER AND 100HZ POWER RIPPLE FROM THE SEQUENCE NETWORK

V	I	P (dc)	$\dot{P}_{100}$ (@100 Hz)
1	1	$\frac{3}{2}V_1I_1\cos(\theta_{v1}-\theta_{i1})$	0
2	2	$\frac{3}{2}V_2I_2\cos(\theta_{v2}-\theta_{i2})$	0
2	1	0	$-j\frac{3}{2}\dot{V}_2\dot{I}_1$
1	2	0	$-j\frac{3}{2}\dot{V}_1\dot{I}_2$
0	1	0	0
0	2	0	0

$$p(t)=\begin{bmatrix}v_a(t)\\v_b(t)\\v_c(t)\end{bmatrix}^T\begin{bmatrix}i_a(t)\\i_b(t)\\i_c(t)\end{bmatrix}$$
$$=V_0(t)^T I_1(t)+V_0(t)^T I_2(t)+V_1(t)^T I_1(t)+V_1(t)^T I_2(t) \quad (11)$$
$$+V_2(t)^T I_1(t)+V_2(t)^T I_2(t)$$

There are six components in (11), and their contributions can be summarized in TABLE II. TABLE II shows that p_{100} is generated by coupling the positive and negative sequence. When connected with a balanced 3-ϕ supply, no negative-sequence voltage and current exist so p_{100} is zero.

A 1-ϕ supply can be considered as an unbalanced 3-ϕ supply, whereas the 3-ϕ voltages and the 3-ϕ currents are as (12):

$$\begin{cases}\left[\dot{V}_{ga},\dot{V}_{gb},\dot{V}_{gc}\right]=\left[\dot{V}_g,0,0\right]\\ \left[\dot{I}_{ga},\dot{I}_{gb},\dot{I}_{gc}\right]=\left[\dot{I}_g,-\dot{I}_g,0\right]\end{cases} \quad (12)$$

By using the *abc*/*zpn* transformation, the voltages and currents in the sequence network can be expressed as (13):

$$\begin{cases}\left[\dot{V}_{g0},\dot{V}_{g1},\dot{V}_{g2}\right]=T_{abc2zpn}\left[\dot{V}_{ga},\dot{V}_{gb},\dot{V}_{gc}\right]=\frac{1}{3}\dot{V}_g\left[1,1,1\right]\\ \left[\dot{I}_{g0},\dot{I}_{g1},\dot{I}_{g2}\right]=T_{abc2zpn}\left[\dot{I}_{ga},\dot{I}_{gb},\dot{I}_{gc}\right]=\frac{1}{\sqrt{3}}\dot{I}_g\left[0,1\angle-30^\circ,1\angle30^\circ\right]\end{cases} \quad (13)$$

where $T_{abc2zpn}=\frac{1}{3}\begin{bmatrix}1&1&1\\1&\alpha&\alpha^2\\1&\alpha^2&\alpha\end{bmatrix}$ is the matrix to compute the sequence components (positive, negative, and zero) from 3-ϕ abc system, and $\alpha=1\angle-30^\circ$ is the complex operator for the $2\pi/3$ rotation.

Substituting (13) into TABLE II derives (14) which is the expression of $\dot{P}_{100-vg}$ (the phasor of the double-line frequency power pulsation generated by the grid) in form of sequence network:

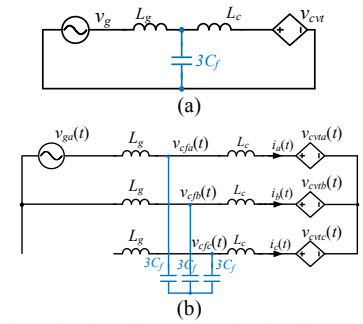

Fig. 7. The equivalent circuits with a 3-ϕ and 1-ϕ grid: (a) the 1-ϕ equivalent circuit with a 3-ϕ grid, and (b) the equivalent circuit with a 1-ϕ grid.

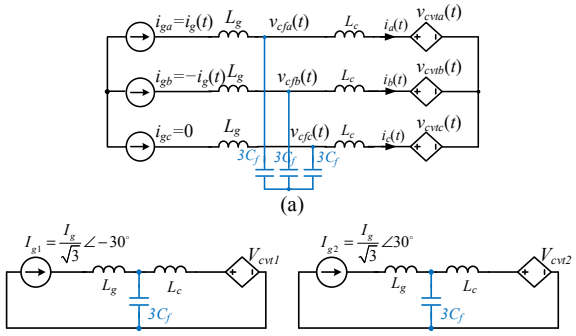

Fig. 8. The equivalent circuits with a 1-ϕ grid: (a) the equivalent circuit with current sources, (b) positive-sequence equivalent circuit, and (c) negative sequence equivalent circuit.

$$\dot{P}_{100-vg}=-j\frac{3}{2}\dot{V}_{g2}\dot{I}_{g1}-j\frac{3}{2}\dot{V}_{g1}\dot{I}_{g2}$$
$$=-j\frac{3}{2}\left(\frac{1}{3}\dot{V}_g\right)\left(\frac{1}{\sqrt{3}}\dot{I}_g\angle-30^\circ\right)-j\frac{3}{2}\left(\frac{1}{3}\dot{V}_g\right)\left(\frac{1}{\sqrt{3}}\dot{I}_g\angle30^\circ\right) \quad (14)$$
$$=-j\frac{1}{2}\dot{V}_g\dot{I}_g$$

B. Operating Principles

As concluded in Section II, the AC side APF with capacitors is preferred. The Y/Δ transformation can amplify the equivalent capacitance provided by the *LCL* filter.

When connected with a 3-ϕ supply as shown in Fig. 6 (a), the 3-ϕ s of the converter are balanced. A 1-ϕ equivalent circuit is shown in Fig. 7 (a). Because p_{100} = 0, there is no double-line frequency power pulsation. The voltage phasor of the rectifier is controlled as $\dot{V}_{cvt}=\dot{V}_g+j\omega_g\left(L_g+L_c\right)\dot{I}_g$. The subscript *cvt* donates the voltage generated by the converter (rectifier).

When connected with a 1-ϕ supply as shown in Fig. 6 (b), the equivalent circuit is shown in Fig. 7 (b) where v_{cvta}, $v_{cvtb,}$ and v_{cvtc} are the 3-ϕ voltages of the converter, and v_{cfa}, v_{cfb} and v_{cfc} are the 3-ϕ voltages across the C_f. Both the power supply and impedance are asymmetrical, and the circuit needs to be simplified. By using the superposition theory, the unconnected terminal (Phase-C) is substituted by a current source with the current as zero, i.e. i_{gc} = 0. The Phase-A and Phase-B form the line and neutral of the 1-ϕ where the current is i_g and $-i_g$ respectively as shown in Fig. 8 (a). The sequence network circuits in terms of the forward and backward sequence are

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shown in Fig. 8 (b) and (c) where the positive sequence current is $\dot{I}_{g1}$ and the negative sequence current is $\dot{I}_{g2}$. The controlled voltage of the rectifier at each phase (v_{cvta}, $v_{cvtb,}$ and v_{cvtc}) can be expressed in the positive sequence (i.e. $\dot{V}_{cvt1}$) and the negative sequence (i.e. $\dot{V}_{cvt2}$) as shown in Fig. 8 (b) and (c).

Two requirements need to be satisfied: 1) the $\dot{I}_g$ needs to be controlled as (15), and 2) the capacitor C_f should store all double-line frequency power pulsation generated by the grid, $\dot{P}_{100-Cf} = \dot{P}_{100-vg}$ as (16).

$$\begin{cases} \dot{V}_g - \left(\dot{V}_{cfa} - \dot{V}_{cfb}\right) = j\omega_g 2L_g \dot{I}_g & (15) \\ \dot{P}_{100-Cf} = \dot{P}_{100-Vg} & (16) \end{cases}$$

where $\dot{P}_{100-Cf}$ and $\dot{P}_{100-vg}$ are the double-line frequency power generated by capacitors and the grid respectively.

The $\dot{P}_{100-Cf}$ is derived as (17) from TABLE II:

$$\begin{aligned} \dot{P}_{100-Cf} &= -j\frac{3}{2}\dot{V}_{cf2}\dot{I}_{cf1} - j\frac{3}{2}\dot{V}_{cf1}\dot{I}_{cf2} \\ &= -j\frac{3}{2}\begin{pmatrix} \dot{V}_{cf1}\, j\omega_g\left(3C_f\right)\dot{V}_{cf2} \\ +\dot{V}_{cf2}\, j\omega_g\left(3C_f\right)\dot{V}_{cf1} \end{pmatrix} \\ &= 9\omega_g C_f \dot{V}_{cf1}\dot{V}_{cf2} \end{aligned} \quad (17)$$

Substituting $\begin{bmatrix} \dot{V}_{cfa} \\ \dot{V}_{cfb} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha^2 & \alpha \end{bmatrix} \begin{bmatrix} \dot{V}_{cf0} \\ \dot{V}_{cf1} \\ \dot{V}_{cf2} \end{bmatrix}$ into (15) derives (18), and substituting (17) into (16) derives (19). Consequently, the two requirements are transformed in the form of sequence network:

$$\begin{cases} \left(1\angle 30^\circ\right)\dot{V}_{cf1} + \left(1\angle -30^\circ\right)\dot{V}_{cf2} = \dfrac{1}{\sqrt{3}}\dot{V}_{REC} & (18) \\ \dot{V}_{cf1}\dot{V}_{cf2} = \dfrac{1}{9\omega_g C_f}\dot{P}_{100-vg} = \dfrac{-j}{18\omega_g C_f}\dot{V}_g \dot{I}_g & (19) \end{cases}$$

where $\dot{V}_{REC} = \dot{V}_g - j\omega_g 2L_g \dot{I}_g$ is a defined vector.

There are two variables ($\dot{V}_{cf1}$ and $\dot{V}_{cf2}$) in the two equations,(18) and (19). The solution can be derived as (20):

$$\begin{cases} \dot{V}_{cf1} = \left(\dfrac{1}{\sqrt{3}}\dot{V}_{REC} \pm \dot{\Lambda}\right)\left(\dfrac{1}{2}\angle -30^\circ\right) \\ \dot{V}_{cf2} = \left(\dfrac{1}{\sqrt{3}}\dot{V}_{REC} \mp \dot{\Lambda}\right)\left(\dfrac{1}{2}\angle 30^\circ\right) \end{cases} \quad (20)$$

where $\dot{\Lambda} = \sqrt{\dfrac{\dot{V}_{REC}^2}{3} - \dfrac{4\dot{P}_{100-vg}}{9\omega_g C_f}}$ is a defined vector.

From Fig. 8 (b) and (c), the rectifier voltage in the positive and negative sequences need to be controlled as:

$$\begin{cases} \dot{V}_{cvt1} = \dot{V}_{cf1} + \left(\dot{V}_{cf1}\, j\omega_g\left(3C_f\right) - \dfrac{\dot{I}_g}{\sqrt{3}}\angle -30^\circ\right) j\omega_g L_c \\ \dot{V}_{cvt2} = \dot{V}_{cf2} + \left(\dot{V}_{cf2}\, j\omega_g\left(3C_f\right) - \dfrac{\dot{I}_g}{\sqrt{3}}\angle 30^\circ\right) j\omega_g L_c \end{cases} \quad (21)$$

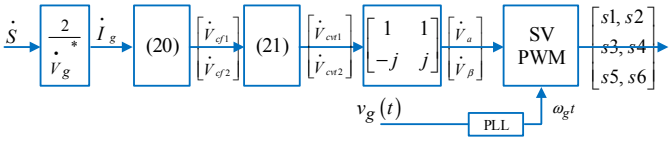

Fig. 9. The open-loop control block for the 1-ϕ connection.

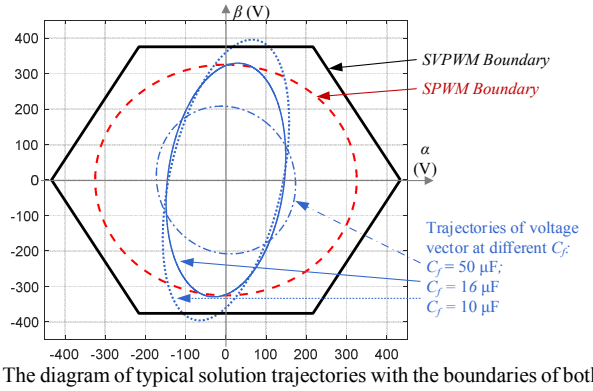

Fig. 10. The diagram of typical solution trajectories with the boundaries of both SPWM and SVPWM (V_{dc} = 650V, P_{100} = 3.3kW).

In order to increase the DC voltage utilization, the SVPWM is used, in which the voltage reference in the $\alpha\beta$ axis is required as :

$$\begin{bmatrix} \dot{V}_{cvt\alpha} \\ \dot{V}_{cvt\beta} \end{bmatrix} = T_{abc2\alpha\beta} T_{zpn2abc} \begin{bmatrix} \dot{V}_{cvt0} \\ \dot{V}_{cvt1} \\ \dot{V}_{cvt2} \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ -j & j \end{bmatrix} \begin{bmatrix} \dot{V}_{cvt1} \\ \dot{V}_{cvt2} \end{bmatrix} \quad (22)$$

where $T_{abc2\alpha\beta} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}$ and $T_{zpn2abc} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha^2 & \alpha \\ 1 & \alpha & \alpha^2 \end{bmatrix}$ are the matrix to performs the *zpn* to *abc* transformation, and the *abc* to $\alpha\beta$ transformation respectively.

Therefore, the open-loop control of this unbalanced operation for a 1-ϕ connection can be illustrated in Fig. 9. With setting the complex power $\dot{S}$, the sequence network voltages on the C_f, the sequence network voltages on the converter, and the converter voltage in the $\alpha\beta$ axis are derived, and the switching signals are generated with SVPWM modulation block.

Fig. 10 shows the trajectory of the required rectifier voltage by using the technique in Fig. 9. Because the rectifier is operating in an unbalanced condition, the trajectory is not a circle but an ellipse. Because the SVPWM is applied, the

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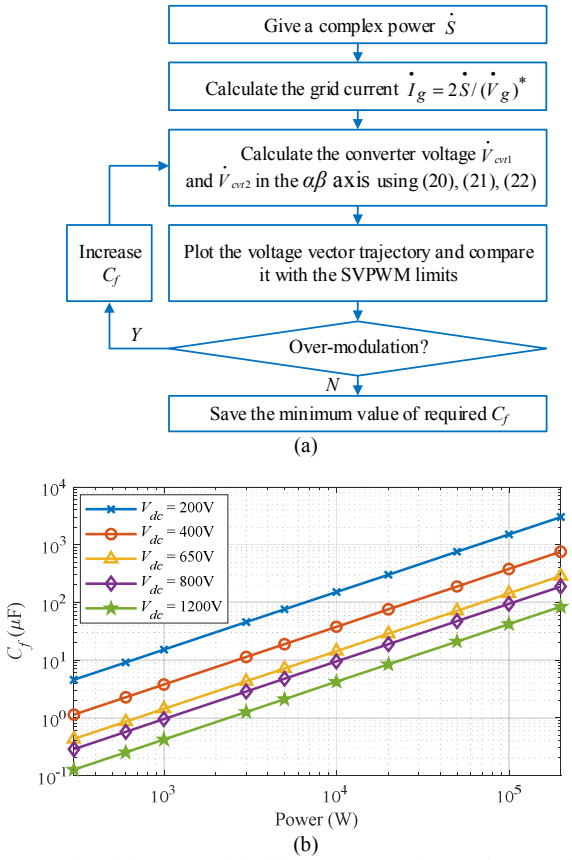

Fig. 11. The minimum C_f with different power ratings and V_{dc} (modulation index = 1): (a) the flowchart of deriving the minimum C_f and (b) the derived minimum C_f.

TABLE III
LCL PARAMETERS FOR THE SYSTEM BY USING THE DESIGN TECHNIQUE IN [43]

S (kVA)	f_g (Hz)	f_{sw} (Hz)	V_g (V rms)	V_{dc} (V)	L_g (mH)	L_c (mH)	C_f (μF)
200	60	20 k	480	1200	0.27	0.1	10
10	50	50 k	380	650	0.336	0.430	0.95

modulation range is increased by 15% compared with the conventional SPWM techniques thus, without increasing the DC-link voltage, the required voltage can be fully covered with a useful margin for other possible grid connection requirements such as voltage fluctuation and reactive power provision.

IV. PARAMETER DESIGN FOR *LCL* FILTER & DC CAPACITOR

A. LCL Filter Design and Size/weight Evaluation

The *LCL* filter, as shown in Fig. 6, comprises the capacitor C_f, the grid-side inductor L_g, and the converter-side inductor L_c. Three requirements of parameters in the *LCL* need to be met for achieving both harmonics filtering and APF functions: 1) storage of the double-frequency power pulsation p_{100}; 2) limitation of the converter side ripple current I_c, and 3) Compliance with the grid code [42] of the grid side current I_g.

The size of C_f is determined by the value of p_{100} and the capacitor voltage. Due to unbalanced operation, the maximum voltage of the capacitor is possibly larger than the peak value of the 1-ϕ supply voltage.

For a fixed DC-link voltage, the capacitor maximum voltage can be located at the trajectory of the AC voltage as shown in Fig. 10. To ensure linear modulation, the elliptical trajectory of the unbalanced voltage must be within the boundary of the circular trajectory of balanced voltage. If C_f is too small, the elliptical trajectory would exceed the circular boundary, resulting in non-linear modulation; if C_f is too large, the modulation index would be small, so the dc voltage utilization is compromised. As shown in Fig. 10, the SVPWM increases the inverted AC voltage by about 15% than the SPWM due to higher DC-link voltage utilization, meaning smaller C_f when using SVPWM or additional voltage margin if the same C_f.

Fig. 11(a) shows the procedure to derive the required minimum C_f to avoid over-modulation under the premise of satisfying eqs. (18) and (19). As shown in Fig. 11(b), C_f increases with the increase of the power rating. The capacitance value of C_f can be then defined by the voltage shown in Fig 10 and the power shown in Fig. 11(b).

The ripple current requirement (i.e. the requirement 2) needs the converter side inductor L_c to satisfy the limit of the current ripple required by the converter. The equation for the inductance calculation is given in [43] and shown as (23).

$$L_c \geq \frac{V_{DC}}{6 f_{sw} \Delta I_{\max}} \tag{23}$$

where f_{sw} is the switching frequency and the ΔI_{max} is the maximum ripple current allowed at the converter circuit.

The grid current requirement (i.e. the requirement 3) is met by achieving the harmonics attenuation, which is calculated by using the transfer function of the *LCL* filter. The largest grid harmonic appears when the 1-ϕ grid is connected (see Appendix), giving the transfer function of the *LCL* filter for 1-ϕ connection:

$$G_{LCL-har}(s) = \frac{I_{g-har}(s)}{V_{cvt-har}(s)} = \frac{2}{s^3 L_g L_c (3C_f) + s(L_g + L_c)} \tag{24}$$

Since f_{sw} is much larger than the resonant frequency between the capacitor and inductor in the *LCL* filter, then $s^3 L_g L_c C_f \gg s(L_g+L_c)$. Therefore, $G_{LCL}(s)$ can be simplified as (25) at f_{sw} :

$$G_{LCL-har}(s) \approx \frac{2}{s^3 L_g L_c (3C_f)} \tag{25}$$

where $V_{har}(s)$ is the harmonic voltage of the converter, and $I_{har}(s)$ is the harmonic current injected to the grid.

The closed-form expressions of the switching harmonic voltages are derived in [44], showing that the most significant harmonic has the frequency f_{sw}. The magnitude of the most significant harmonic in a half-bridge is:

$$V_{har} = \frac{2V_{dc}}{\pi} J_0\left(\frac{\pi}{2} M\right) \leq \frac{2V_{dc}}{\pi} \tag{26}$$

where V_{har} is the most significant harmonic's magnitude, J_0 is the first-order Bessel function and is always smaller than 1; M is the modulation index within [0, 1]. When $M = 0$, V_{har} reaches its maximum value.

$$I_{har} = V_{har} G_{LCL-har}(s = j\omega_{sw}) \leq I_{std} \tag{27}$$

TABLE IV
VOLUME/WEIGHT COMPARISON OF THE *LCL* FILTER BETWEEN DESIGNED VALUES AND VALUES IMPLEMENTED WITH COMMERCIALIZED DEVICES FOR THE CONVENTIONAL OBC WITH K_{Cf}= 1

	Designed parameters	Selected devices	Energy capacity (J) (r3)		Evaluated volume (mm³) (r4)		Evaluated weight (g) (r5)		Actual volume (mm³)	Actual weight (g)
			Designed parameters	Selected devices	Designed parameters	Selected devices	Designed parameters	Selected device		
L_c	336 μH @ 28 A	*7443763540470* (r1) × 7 (329 μH, 31 A)	0.1310	0.1581	2.62×10^5	3.16×10^5	1310	1720	3.62×10^5	1568
L_g	430 μH @ 28 A	*7443763540470* × 9 (423 μH, 31 A)	0.1673	0.2033	3.35×10^5	4.06×10^5	1670	2202	4.65×10^5	2016
C_f	0.9 μF @ 845V	*MKP1848510094K2* (r2) (1 μF, 900V)	0.3418	0.4050	3418	4050	3.4	4.1	5472	6.0

(r1) *7443763540470* is an inductor from Wurth Electronics Inc, and its volume/weight is 51660 mm³ / 224.0 g.
(r2) *MKP1848510094K2* is a film capacitor from Vishay, and its volume/weight is 5472 mm³ / 6 g.
(r3) Energy capacity equals $0.5LI^2$ for inductors and $0.5CV^2$ for capacitors. For instances, the energy capacity of L_c with designed parameters is 0.5 × 336 μH × (28 A)² = 0.1311 J; the energy capacity of L_c implemented with selected devices is 0.5 × (47 μH × 7) × (31 A)² = 0.1581 J.
(r4) Eq. (1) shows that VOL_L = energy capacity / K_{VL}; eq. (2) shows that VOL_C = energy capacity / K_{VC}. $K_{VL} \approx 5\times10^{-7}$ J/mm³ and $K_{VC} = 1\times10^{-4}$ J/mm³ can be extracted from Fig. 3.
(r5) The two coefficients $K_{WL} \approx 1\times10^{-4}$ J/g and $K_{WC} = 0.1$ J/g from Fig. 3 are used to evaluate the weight.

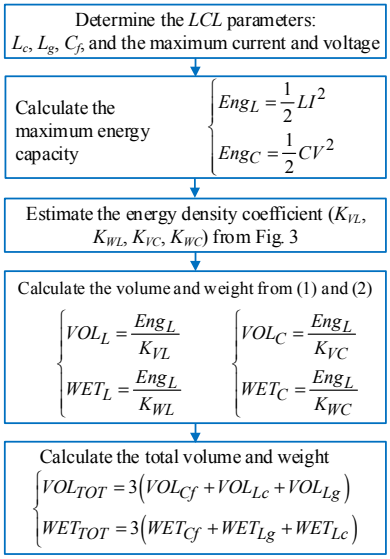

Fig. 12. The flow-chart to evaluate the volume/weight of the *LCL* filter.

where I_{std} is the maximum harmonic limit in the grid code. This paper applies IEEE Std 519 [42] as the grid limits in which I_{std} = 0.3%I_{rated} when $f_{sw} > 35f_g$.

From (26) and (27), the minimum value of L_g is derived as:

$$L_g \geq \frac{4V_{dc}}{\pi\omega_{sw}{}^3 L_c \left(3C_f\right) I_{std}} \tag{28}$$

Fig. 11, (23) and (28) can be used to determine C_f, L_c, and L_g respectively. The proposed technique requires larger C_f than the existing design because the value of C_f is determined by voltage modulation and energy storage given by Fig. 10 and Fig. 11. In this paper, the DC-link voltage needs to be regulated at 650 V which is commonly used in OBCs and the 1-ϕ power rating is set to be 10 kW, which covers the common 6.6 kW and 3.3 kW Level 2 and Level 1 charging standards.

The required C_f is 14.3 μF obtained from Fig. 11, which is larger than 0.95 μF of the conventional method in [43]. However, (28) shows that the increase of C_f can lead to a decrease of L_g. The total volume and weight of the *LCL* filter need to be assessed.

Denoting K_{Cf} as the coefficient of quantifying the increase of C_f, considering L_c remains unchanged from (23), then L_g is decreased by K_{Cf} from (28). The volume and weight of the *LCL* filter are functions of K_{Cf}, and can be expressed as (29) and (30) respectively:

$$\begin{cases} VOL_{TOT}\left(K_{Cf}\right) = 3\left(K_{Cf} \bullet VOL_{Cf} + VOL_{Lg}/K_{Cf} + VOL_{Lc}\right) \\ WET_{TOT}\left(K_{Cf}\right) = 3\left(K_{Cf} \bullet WET_{Cf} + WET_{Lg}/K_{Cf} + WET_{Lc}\right) \end{cases} \tag{29, 30}$$

where VOL_{TOT}, VOL_{Cf}, VOL_{Lg} and VOL_{Lc}, WET_{TOT}, WET_{Cf}, WET_{Lg}, and WET_{Lc} are the volume and weight of *LCL* filter, C_f, L_g, and L_c respectively.

In order to compare with the *LCL* design from [43] which was for 200 kVA, the *LCL* filter is recalculated by using the same method in [43] to compare with the filter used in this proposed method at 10 kVA, 650 V DC-link system. The *LCL* parameters of the conventional method in [43] at 200 kVA and 10 kVA are shown in TABLE III, and its volume/weight can be evaluated with Fig. 12. For the 200 kVA system [43], L_c= 100 μH, L_g= 270 μH, C_f= 10 μF; the rated current and voltage are 240 A (rms) and 1200 V (peak). If a 30% margin is used for the inductor current and capacitor voltage, the required maximum energies stored in L_c, L_g, and C_f are Eng_{Lc} = $0.5L_g$ $(1.3\times\sqrt{2}\times240)^2$ J = 9.78 J, $Eng_{Lg} = 0.5L_c(1.3\times\sqrt{2}\times240)^2$ J = 26.4 J and $Eng_{Cf} = 0.5C_f\,(1.3\times1200)^2$ = 12.2 J. Their volume and weight can be evaluated with the energy density equation in (1). In [43], L_g used silicon steel inductors where $K_{VL} \approx 10^{-6}$ J/mm³ and $K_{WL} \approx 2\times10^{-4}$ J/g, giving $VOL_{Lg} = Eng_{Lc} / K_{VL} = 26.4\times10^6$ mm³ and $WET_{Lg} = = Eng_{Lc} / K_{WL} = 132\times10^3$ g; L_c used nanocrystalline based inductor, and the volume is given as $VOL_{Lc} = 6.78\times10^6$ mm³ in [43], and $WET_{Lc} = VOL_{Lc} / density = 34\times10^3$ g when $density \approx K_{VL} / K_{WL} = 5.0$ g/cm³; C_f used film capacitors where $K_{VC} \approx 10^{-4}$ J/mm³, $K_{WC} \approx 0.1$ J/g, and $VOL_{Cf} = 121\times10^3$ mm³, giving WET_{Cf} = 121 g. Therefore, the total volume and weight for the system with K_{Cf} = 1 can be derived as: $VOL_{TOT}(K_{Cf} = 1) = 9.99\times10^8$mm³; $WET_{TOT}(K_{Cf} = 1) = 4.98\times10^5$ g.

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From Fig. 13(a), the optimal volume can be achieved when K_{Cf} = 15.25. From (23), L_c remains unchanged; from (29) and (30), L_g is decreased to (270 μH / K_{Cf}) = 17.7 μH and C_f is increased to (10 μF × K_{Cf}) = 153 μF. From (29) and (30), the total volume and weight are $VOL_{TOT}(K_{Cf}$ = 15.25) = 3.11× 10^7 mm^3 and $WET_{TOT}(K_{Cf}$ = 15.25) = 1.33×10^5 g, respectively. Similarly, from Fig. 13(b), the optimal weight can be achieved when K_{Cf} = 31.50. From (23), L_c remains unchanged; from (29) and (30), L_g is decreased to 270 μH / K_{Cf} = 8.57 μH and C_f is increased to 10 μF × K_{Cf} = 315 μF. According to (29) and (30), the total volume and weight are $VOL_{TOT}(K_{Cf}$ = 15.25) = 3.4× 10^7 mm^3 and $WET_{TOT}(K_{Cf}$ = 15.25) = 1.3×10^5 g, respectively.

The total volume and weight of the *LCL* filter can be plotted by using (28) and (29) as illustrated in Fig. 13. It is clearly shown that the design in [43] can be improved by increasing K_{Cf} so the total volume and weight of the *LCL* filter can be decreased. The optimal K_{Cf} for the total volume and weight can be calculated by setting the first derivatives to be zero as $\frac{d(VOL_{TOT})}{dK_{VOL}}=0$ and $\frac{d(WET_{TOT})}{dK_{VOL}}=0$. The solutions are:

$$K_{Cf}\big|_{\text{opt vol}}=\sqrt{\frac{VOL_{Lg}}{VOL_{Cf}}} \tag{31}$$

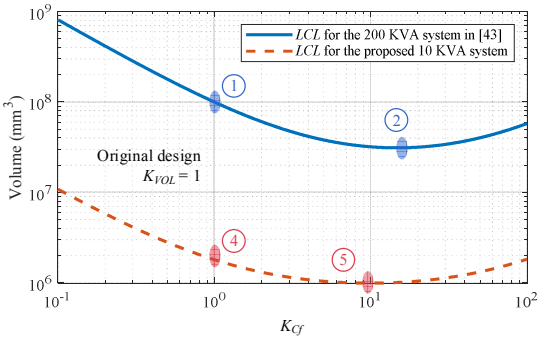
$$K_{Cf}\big|_{\text{opt wet}}=\sqrt{\frac{WET_{Lg}}{WET_{Cf}}} \tag{32}$$

where $K_{Cf}\big|_{\text{opt vol}}$ and $K_{Cf}\big|_{\text{opt wet}}$ are the K_{Cf} for the optimal volume and the optimal weight respectively.

When (31) is met, $K_{Cf}VOL_{Cf}=VOL_{Lg}/K_{Cf}$, which means that the when C_f and L_g have the same volume, the optimal volume can be reached. Similarly, when the C_f and L_g have the same weight, (32) is met and the optimal weight can be reached. In the conventional design, both the volume and weight of L_g is much larger than C_f due to a small capacitance of C_f. However, in this proposed design, the increased capacitance C_f will enable the volume and weight of the C_f and L_g become closer to each other, thus the total volume and weight of the filter will become closer to the optimum.

For S = 10 kVA with the *LCL* designed technique in [43], the parameters can be derived as the marker 4 of Fig. 13(c): L_c, L_g, and C_f are 336 μH at 21.5 A, 420 μH at 21.5 A and 0.96 μF at 650 V, respectively. If a 30% margin is used for the inductor current and capacitor voltage, the currents for both L_c and L_g are 28.0 A, and the voltage for C_f is 845 V. Thus, the energy stored in L_c, L_g, and C_f are Eng_{Lc}= 0.5 × 336 μ ×28^2 = 0.1311 J, Eng_{Lg} = 0.5 × 336 μ ×28^2 = 0.1673 J, and Eng_{Cf}= 0.5 × 0.9 μ × 845^2 = 0.3418 J, respectively. If both L_c and L_g use inductors with MPP cores with K_{VL} ≈ 5×10^{-7} J/mm^3, and K_{WL} ≈ 1×10^{-4} J/g as shown in Fig 1, the volume and weight are of inductors are: VOL_{Lc} = 2.62×10^5 mm^3, WET_{Lc} = 1.31×10^3 g, VOL_{Lg} = 3.34×10^5 mm^3, WET_{Lg} = 1.67×10^3 g. For C_f, K_{VC} = 1×10^{-4} J/mm^3, K_{WC} = 0.1 J/g, Eng_{Cf} = $0.5CV^2$ = 0.3418 J, therefore, VOL_{Cf} = Eng_{Cf}/K_{VC} = 0.3418 / 1×10^{-4} = 3.42×10^3 mm^3, and WET_{Cf} = Eng_{Cf}/K_{WC} = 0.3418 / 0.1 = 3.42 g.

To verify the designed effectiveness of the designed value, TABLE IV is added to compare the weight and volume between



	System in [43]			The proposed system			
Marker	①	②	③	④	⑤	⑥	⑦
Comment	Existing value in [43]	Optimal Volume	Optimal Weight	Value based [43]	Optimal Volume	Optimal Weight	p_{100}: C_f= 16 μF
K_{Cf}	1.00	15.25	31.50	1.00	10.28	22.93	16.67
VOL_{TOT} (mm^3)	9.99×10^8	3.11×10^7	3.4×10^7	1.80×10^6	9.90×10^5	1.07×10^6	1.02×10^6
WET_{TOT} (g)	4.98×10^5	1.33×10^5	1.3×10^5	8964	4528	4388	4406
L_c (μH)	100	100	100	336	336	336	336
L_g (μH)	270	17.7	8.57	430	41.8	18.8	25.8
C_f (μF)	10	153	315	0.96	9.89	22	16

(c)

Fig. 13. The total (a) volume and (b) weight of the *LCL* filter versus K_{Cf}, and (c) the specific parameters from the above figures. The blue curves / markers / data are for the 200 kVA system in [43]; the red curves / markers / data are for the 10 kVA system.

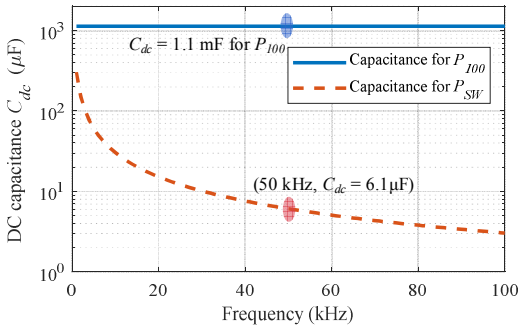


Fig. 14. The required DC capacitance comparison between p_{100} and P_{SW}. P_{dc} = 3 kW, V_{dc} = 650 V, ΔV_{dc}= 13 V (2% of V_{dc}).

the designed parameters and the commercial devices. The evaluated volume and weight are 1.8×10^6 mm^3 and 8.95×10^3 g; the volume and weight of actual commercial components are 1.8×10^6 mm^3 and 8.95×10^3 g. The differences between evaluation and actual devices are small as shown in Table IV . It should be noted that the weight and volume differences on

the capacitor C_f between evaluation and actual device are more significant than that from the inductors. However, the capacitor is much smaller and lighter than the inductor thus this deviation between evaluation and actual commercial components can be neglected in the *LCL* filter design.

Fig. 13 clearly shows that volume and weight can be decreased with increased K_{Cf}. The *LCL* filter reaches the optimal volume and weight when K_{Cf} = 10.28 and 22.93 respectively. If C_f is set as 16 μF in this proposed method, then K_{Cf} = 16.67, VOL_{TOT} = 1.02×10^6 mm^{3}and WET_{TOT} = 4406 g, which are closer to the optimum. The volume and weight of the *LCL* filter with K_{Cf} = 16.67 (the marker 7 in Fig. 13) can be reduced by 76.47% and 103.4% respectively compared to the conventional design with K_{Cf} = 1 (the marker 4 in Fig. 13).

In conclusion, although the proposed technique requires that the *LCL* filter not only attenuates the harmonic current to the grid but also store the double-line frequency power pulsation, both the size/weight of the *LCL* filter can be reduced with the proposed technique because the increased capacitance C_f for storage has moved the total volume and weight closer to the optimum as shown in Fig. 13.

B. Parameter Design for the DC-Link Capacitor

For the conventional 1-ϕ HB converter, the capacitance required to smooth the 100 Hz power pulsation is given as [45]:

$$C_{dc} > \frac{P_{dc}}{(2\omega_g)V_{dc}\left(\frac{1}{2}\Delta V_{dc}\right)} = \frac{P_{dc}}{\omega_g V_{dc}\Delta V_{dc}} \tag{33}$$

The proposed APF technique can eliminate the double-line frequency power pulsation. Therefore, the switching harmonics determine the DC capacitance.

The closed-form expressions of the switching harmonic voltages in [44] show that the most significant harmonics locates at the switching frequency f_{sw}. The magnitude of the most significant harmonic is:

$$V_{sw} = \frac{2V_{dc}}{\pi}J_0\left(\frac{\pi}{2}M\right) \le \frac{2V_{dc}}{\pi} \tag{34}$$

where J_0 is the Bessel function of the first kind, and M is the modulation index. When M = 0, V_{SW} reaches its maximum value.

If the AC output voltage and current are: $v_{sw}(t)$ = $V_{sw}\sin(\omega_{sw}t+\theta_{swu})$ and $i_{sw}(t)$ = $I_{sw}\sin(\omega_{sw}t+\theta_{swi})$, where θ_{swu} and θ_{swi} are the initial phase of $v_{sw}(t)$ and $i_{sw}(t)$. The instantaneous power at the AC output is $p(t)$ = $(V_g\sin(\omega_g t)$ + $V_{sw}\sin(\omega_{sw}t+\theta_{swu}))\times(I_g\sin(\omega_g t)$ + $I_{sw}\sin(\omega_{sw}t+\theta_{swi}))$. Because I_{sw} needs to be smaller than 4% of the grid current I_g to comply with the grid code [42], it can be neglected. Therefore, the expression of $p_{sw}(t)$ and its magnitude P_{SW} are:

$$\begin{cases} p_{sw}(t) \approx V_{sw}I_g sin(\omega_g t)sin(\omega_{sw}t+\theta_{swu}) \\ P_{SW} = \frac{1}{2}V_{sw}I_g \end{cases} \tag{35}$$

Because the semiconductors do not store energy, P_{SW} also donates the magnitude of the instantaneous power at the DC-link. The P_{SW} for an unbalanced 3-ϕ converter is three times smaller than that in a half-bridge. The required capacitance needs to meet:

$$C_{dc} > \frac{3P_{sw}}{\omega_{sw}V_{dc}\left(\frac{1}{2}\Delta V_{dc}\right)} = \frac{6P_{sw}}{\omega_{sw}V_{dc}\Delta V_{dc}} \tag{36}$$

Fig. 14 shows the comparison of the required DC capacitance for the P_{SW} at switching frequency and for the p_{100} at the double-line frequency. The C_{dc} for P_{SW} is significantly smaller than the C_{dc} for p_{100}, especially for the applications with a large f_{sw}. Because the proposed technique only needs C_{dc} for P_{SW}, the size and volume can be greatly reduced. For f_{sw} = 50 kHz, $C_{dc} \ge$ 6.1 μF, and a 10 μF capacitor is used for C_{dc} in this paper.

TABLE V
CIRCUIT PARAMETERS

Grid voltage V_g	230 V (RMS, 1-ϕ) 400 V (RMS, 3-ϕ)
Grid frequency f_g	50 Hz
Grid side inductor L_g	30 μH
Converter side inductor L_c	350 μH
LCL capacitor C_f	16 μF
DC-link capacitor C_{dc}	10 μF
DC-link voltage V_{dc}	650 V
Output power P_o	3 kW (1-ph) 10 kW (3-ph)
Switching frequency f_{sw}	50 kHz

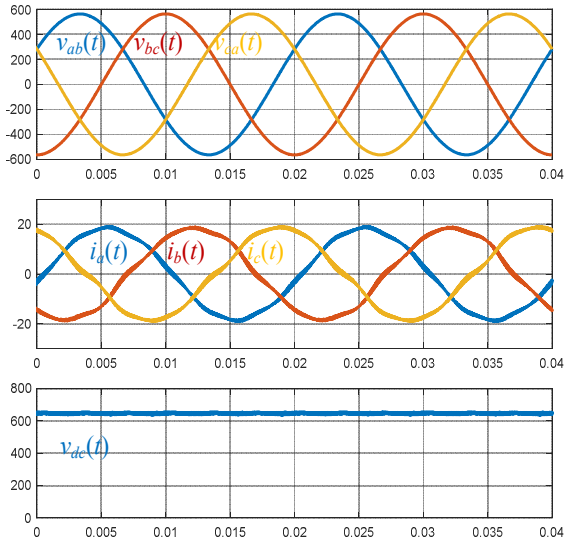


Fig. 15. The simulated waveforms of the converter with 3-ϕ power supply at 400 V and 10 kW. The V_{dc} = 650 V.

V. SIMULATION AND EXPERIMENT RESULTS

A. Simulations

The proposed circuit is shown in Fig. 6, and the parameters are shown in TABLE V. Fig. 15 and Fig. 16 shows the simulation results of the rectifier fed by 1-ϕ supply at 3 kW and 3-ϕ supply at 10 kW respectively. The proposed OBC will have two connectors, the 1-ϕ connector (regulated by BS13363) and the 3-ϕ connector (regulated by IEC 62196), for users to select.

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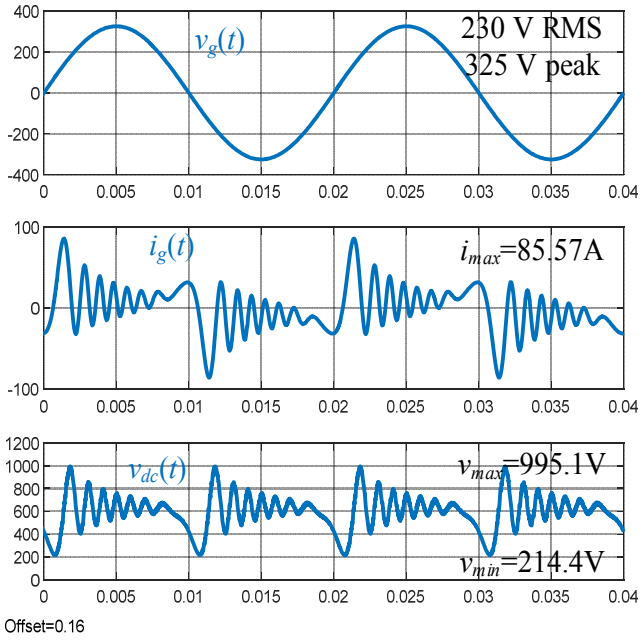
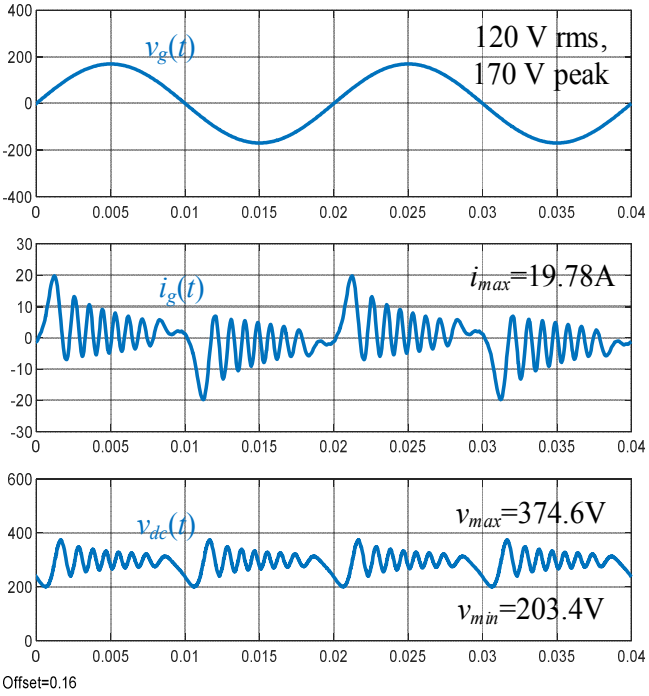


(a)



(b)

Fig. 16. The simulated waveforms of the conventional H-bridge (HB) with the *LCL* filter (all the parameters are as shown in TABLE V) connected to a 1-ϕ grid: (a) V_g = 230V, P_o = 3 kW and (b) V_g = 120 V, P_o = 300 W.

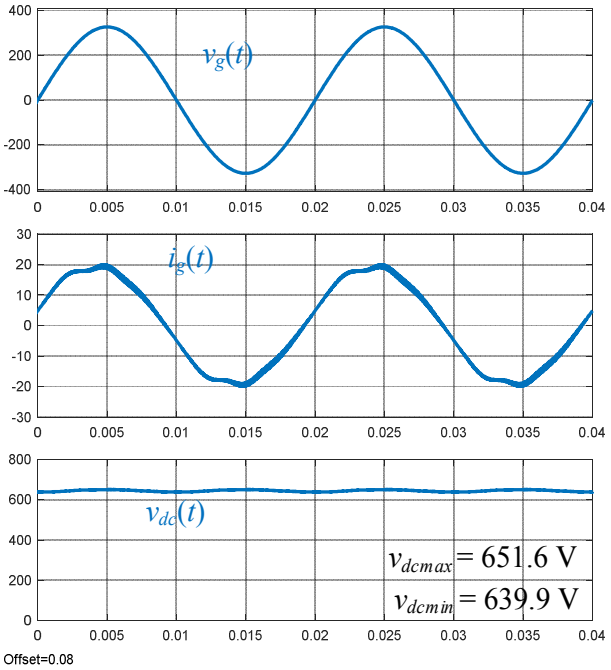
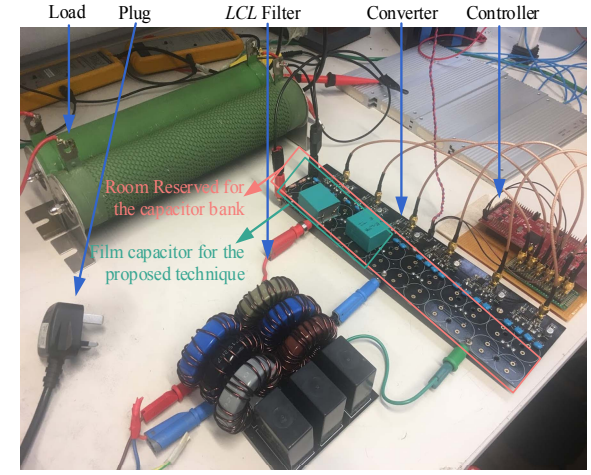


Fig. 17. The simulated waveforms of the proposed method of the converter connected to a 1-ϕ grid.



(a)

W × L × H = 80×275×25 mm^3
Volume = 550×10^{3}mm^3
Weight = 710.6 g
(b)

W × L × H = 31.5×44×37 mm^3
Volume = 51.28×10^3 mm^3
Weight = 66 g
(c)

Fig. 18. Test set-up of (a) overall converter, (b) the capacitor bank for the dc capacitor storage technique, and (c) the film capacitor for the proposed technique.

Once the corresponding plug has been connected, the OBC will work accordingly for that connection, either 1-ϕ or 3-ϕ. It is obvious that the charging voltage remains the same during each charging event, either 1-ϕ or 3-ϕ for each charging event thus there is no need for dynamic switching between 1-ϕ and 3-ϕ within one charging event. However, the additional 3-ϕ charging opportunity offered by the technology reported in this paper will benefit motorists by using 3-ϕ charging facility for three times higher charging rate by using the 1-ϕ and 3-ϕ compatible OBC.

Fig. 15 shows that both the DC-link voltage and the AC line current are smooth when connected with a 3-ϕ grid. The performance of the rectifier with a small DC capacitor and without using the APF is firstly assessed to highlight the significance of the distortion caused by the double-line power

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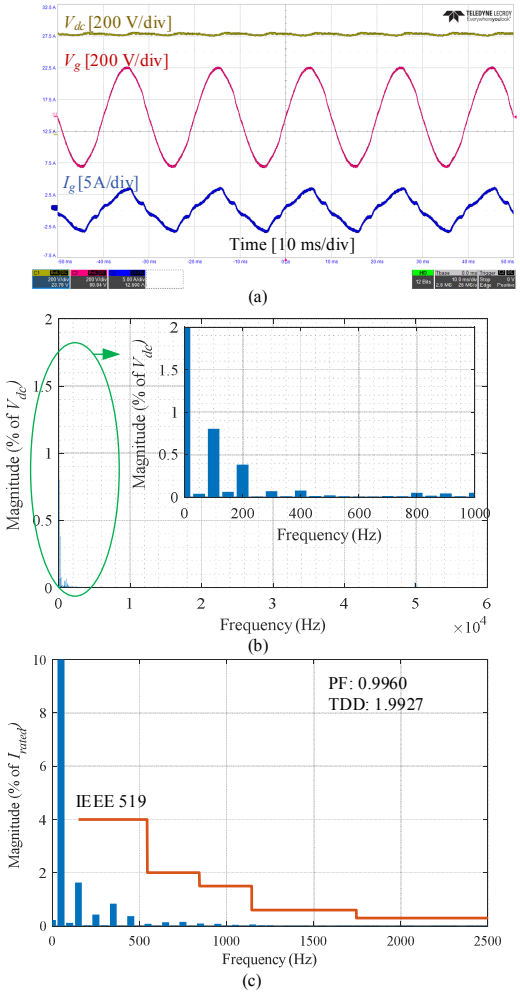

Fig. 19. The 300 W experimental results of the proposed technique with the 10 μF dc capacitor: (a) the waveforms of V_{dc}, V_g, and I_g, (b) the spectrum of the dc voltage V_{dc}, and (c) the spectrum of the grid current I_g versus the IEEE 519 current limit.

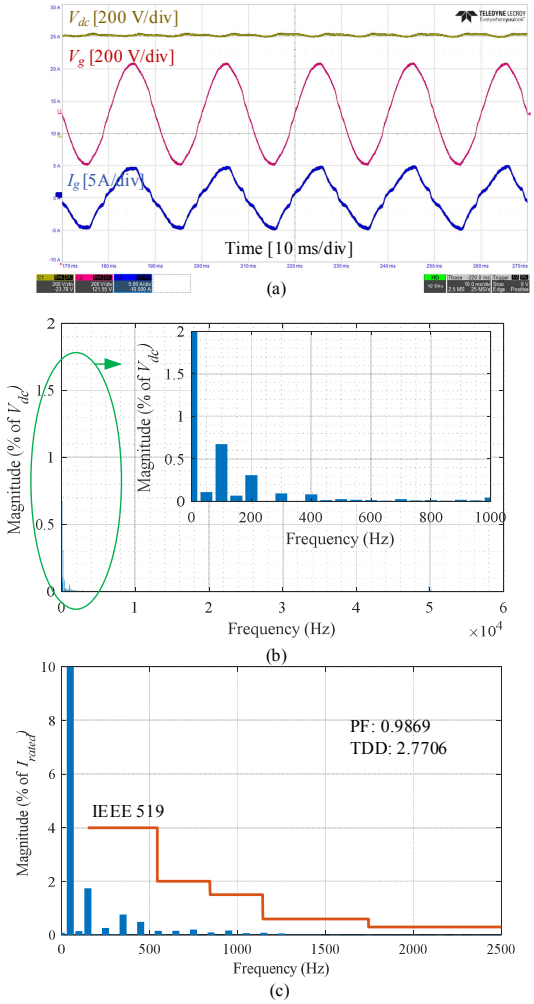

Fig. 20. The 500 W experimental results of the proposed technique with 10 μF dc capacitors: (a) waveforms, (b) dc voltage spectrum, and (c) current spectrum versus standard limit.

pulsation. When connected with a 1-ϕ grid using the conventional 1-ϕ converter (the HB circuit with the *LCL* filter in TABLE V, 10 μF dc capacitor, and the SPWM modulation technique) for the rated 3 kW operation, as shown in Fig. 16 (a), both the DC voltage and the AC current are greatly distorted due to the 100 Hz power pulsation. The voltage ripple is 780.7 V which was more than the nominal DC voltage of 650 V, and the maximum value reaches 95.1 V. The grid current is also significantly distorted because of the DC voltage ripple. Because the voltage and current stress are significantly higher than th e nominal voltage and current and the magnitude of the over current and voltage depend on the power, it is impractical to verify the results with experiment at the rated power if using the same rating of the devices in the rectifier. Instead, a scaled-down test set-up with V_g = 120 V and P_o = 300 W is conducted experimentally thus a 300 W simulation as shown in Fig. 16(b) is also presented for comparison. If the proposed technique with C_{dc} = 10 μF is applied, the DC-link voltage ripple in Fig. 17 is 11.7 V; in comparison, if the conventional HB with C_{dc} = 10 μF is applied, the ripple voltage as shown in Fig. 16(b) is (995.1 − 214.4) V = 780.7 V. The comparison between Fig. 16(b) and Fig. 17 shows that the proposed technique can greatly reduce the 2nd order harmonic in the DC-link. The conventional HB can also achieve small 2nd harmonic with bulk DC capacitors, and the required C_{dc} can be calculated by using (33): to achieve ΔV_{dc} = 11.7 V, the required C_{dc} is C_{dc} = 3000 / (314×650×11.7) F = 1.13 mF; in comparison, to achieve ΔV_{dc} = 11.7 V, Fig. 17 with the proposed technique only uses C_{dc} = 10 μF. Comparing between 10 μF in the proposed technique and the 1.13 mF in the conventional H-bridge converter, it can be concluded that the proposed APF requires only less than 1% capacitance of the DC capacitor to achieve the same 2nd order DC harmonics.

B. Experiments

The experiment test set-up is shown in Fig. 18. The comparison between Fig. 18 (b) and (c) showed that the size reduction of the DC-link capacitor is significant. The significant reduction of the DC capacitance allows using the film capacitors at the DC-link, which improved the reliability and lifetime of the OBC due to higher robustness of the film capacitor than its electrolytic counterpart.

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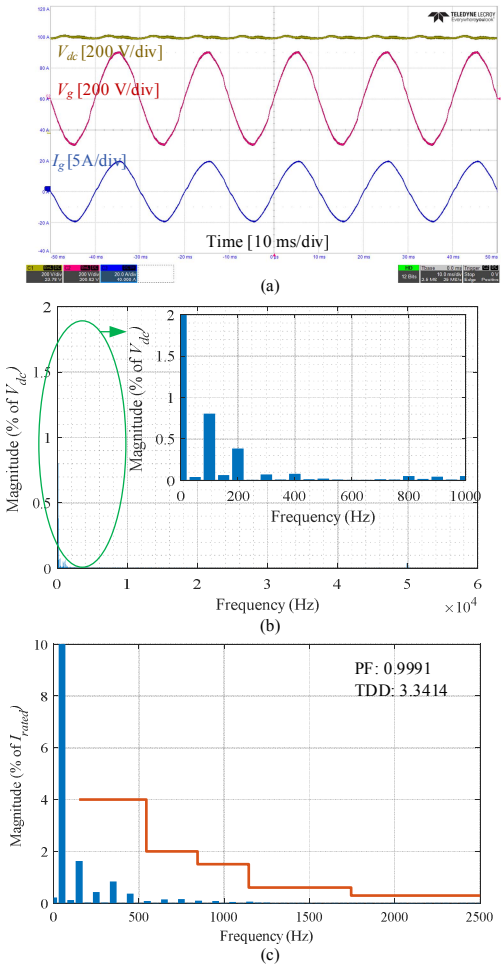

Fig. 21. The 3000 W experimental results of the proposed technique with the 10 μF dc capacitor: (a) the waveforms of V_{dc}, V_g, and I_g, (b) the spectrum of the dc voltage V_{dc}, and (c) the spectrum of the grid current I_g versus the IEEE 519 current limit.

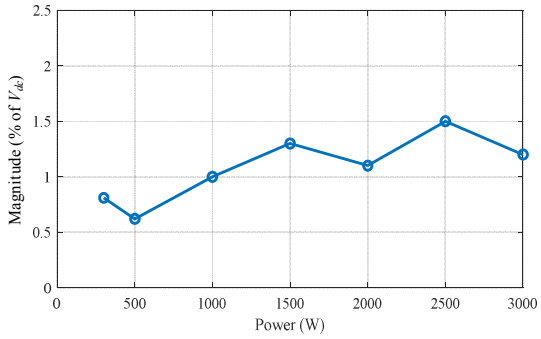

Fig. 22. The percentage of the 100 Hz voltage ripple of V_{dc} over its mean value at various loads with the proposed technique and 10 μF dc capacitor.

Fig. 19-Fig. 21 show the experiments with the proposed APF technique at 300 W, 500 W, and 3 kW rated power respectively. The waveforms in Fig. 19(a), Fig. 20(a) and Fig. 21(a) show that the DC-link voltage was smooth, and the grid current is sinusoidal with acceptable small distortions; the dc ripple spectrum in Fig. 19(b), Fig. 20(b), and Fig. 21(b) show that the 100 Hz voltage pulsations are small at various load conditions; the grid current spectrum show that at various load conditions,

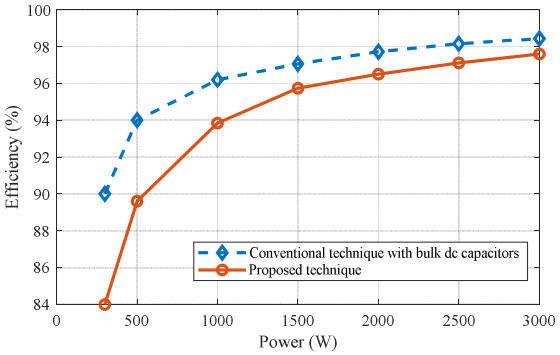

Fig. 23. The experimental efficiency comparison between the proposed technique with 10 μF dc capacitor and the conventional 1-ϕ HB converter with 1.3 mF dc capacitor at various loads.

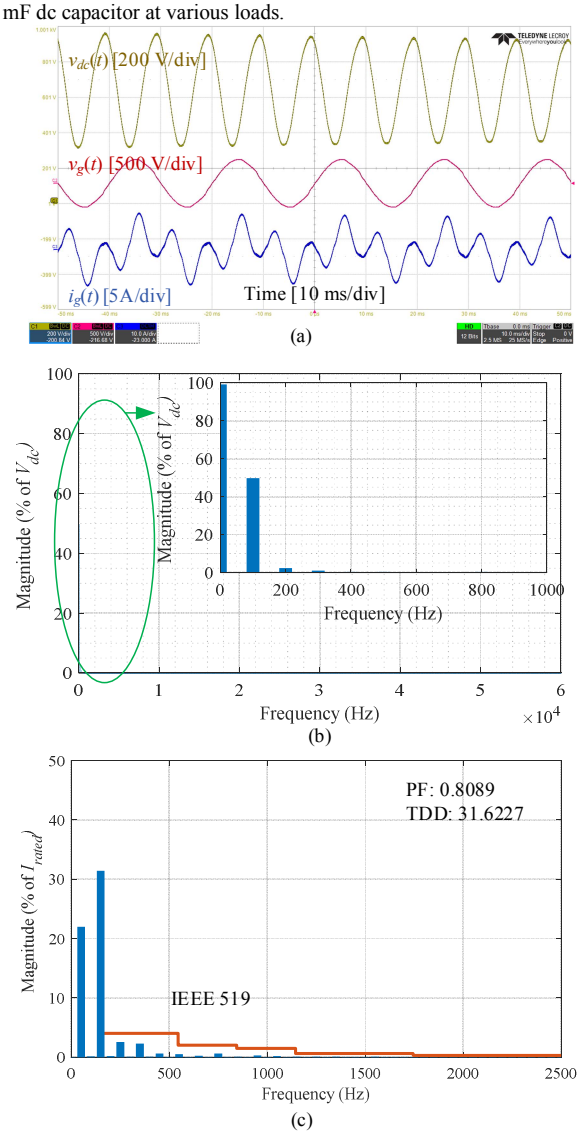

Fig. 24. The 300 W experimental results of the conventional H-bridge converter with the 10 μF dc capacitor: (a) the waveforms of V_{dc}, V_g, and I_g, (b) the spectrum of the dc voltage V_{dc}, and (c) the spectrum of the grid current I_g versus the IEEE 519 current limit.

the grid current can satisfy the grid code in the IEEE 519. The experimental results in Fig. 21 match the simulations shown in Fig. 17 well. Fig. 22 shows that the proposed technique can

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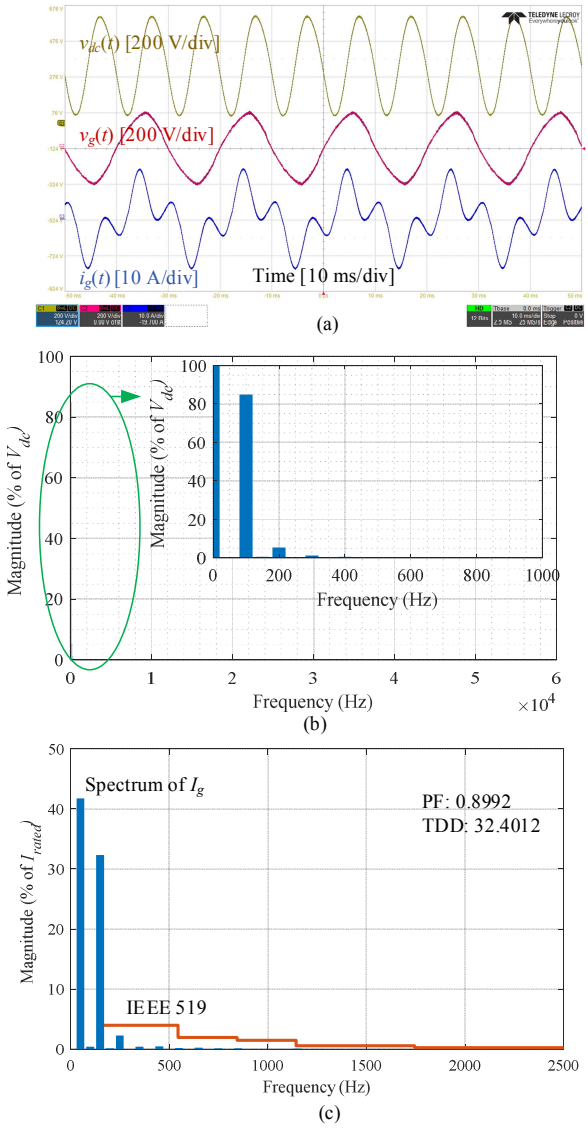

Fig. 25. The 500 W experimental results of the conventional H-bridge converter with the 10 μF dc capacitor: (a) the waveforms of V_{dc}, V_g, and I_g, (b) the spectrum of the dc voltage V_{dc}, and (c) the spectrum of the grid current I_g versus the IEEE 519 current limit.

limit the magnitude of the 100 Hz voltage ripple with the various loads to less than 1.5% of the DC voltage (650V) from 300 W to 3000 W.

Fig. 23 shows the efficiency comparison between the proposed technique with 10 μF dc capacitor and the conventional 1-ϕ converter (the HB circuit with the *LCL* filter in TABLE V, and the SPWM modulation technique) with 1.3 mF dc capacitors. The efficiency of the proposed technique decreases because the extra APF (the third leg) consumes power, and the peak efficiency is 97.6% at 3000 W.

Fig. 24(a) and Fig. 25(a) shows that the conventional 1-ϕ converter (which is a HB with the *LCL* filter) with 10 μF dc capacitance suffered great distortion from both the DC-link voltage and the grid current. When operating at 500W, the experiment of non-APF is conducted with reduced V_g (120 V) and V_{dc} (325 V) to avoid the over voltage / current failure caused by power pulsation. Fig. 24(b) and Fig. 25 (b) shows that the 100 Hz ripple was 49.97% (324.8 V) and 84.89% (275.8 V) respectively. The experiment matched the simulations shown in Fig. 16 (b) well.

VI. Conclusion

This paper proposes a voltage-source converter which is compatible with both 1-ϕ and 3-ϕ grids. The circuit is still the classic 3-ϕ converter, but the control stratagem and the *LCL* filter are redesigned to address the issue of the power pulsation at double-line the grid frequency. When connected with a 1-ϕ grid, the power pulsation at double-line the grid frequency is diverted and stored into the *LCL* filter by utilizing the third leg of the rectifier circuit. Therefore, neither extra active switches nor passive components are required. The advantages of the proposed technology can be summarized as below:

1. Good compatibility: the charger can work with both 3-ϕ and 1-ϕ grids without changing the topology. When connected with a 1-ϕ grid, the third leg is used, and no extra active switches are required.
2. Simple circuit: C_f in the *LCL* filter is utilized to store the pulsating power. L_g and L_c are utilized to damp the ripple current. Therefore, no extra passive components are required.
3. *LCL* filter's size/volume reduction: Although the C_f of the *LCL* filter is increased to store the pulsating power, the total volume and weight of the *LCL* filter can be reduced by 76.47% and 103.4% due to the reduction of the L_g.
4. DC-link capacitance reduction: The DC-link capacitance can be reduced by 130 times at the same switching frequency of the rectifier compared with the conventional DC capacitor storage techniques as mentioned in the experimental section.
5. Unified equations for size evaluation: the unified equations are obtained to identify the optimal circuit for AC/DC APFs with capacitors/inductors as energy storage devices and can be used to optimize the size/weight of the *LCL* filter.
6. High dc-voltage utilization: when connected with a 1-ϕ grid, the system operates in an unbalanced 3-ϕ condition. Therefore, the advantages of the 3-ϕ system can be utilized to increase the DC voltage utilization by 15% and increase the utilization of the *LCL* capacitor by three times because of applying the SVPWM and Y/Δ transformation provided by the 3-ϕ systems.

Appendix
Grid Harmonic Current with 1-Φ Grid

When operating with under 1-ϕ voltage, the circuit is as shown in Fig. 26, which is a 4-node network. Write the nodal equations in the matrix format as follows:

$$\boldsymbol{Y}\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = Y_{Lc}\begin{bmatrix} V_{cvta} \\ V_{cvtb} \\ V_{cvtc} \end{bmatrix}$$

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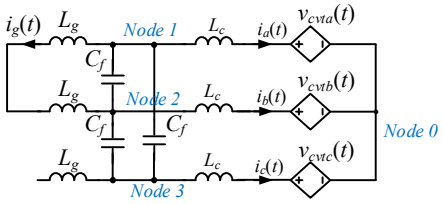

Fig. 26. The equivalent circuit of proposed technique for 1-ϕ grid.

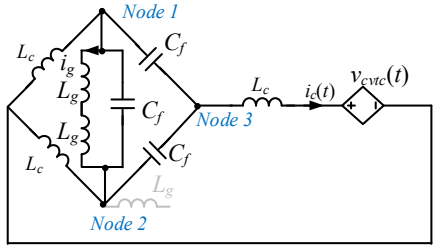

Fig. 27. The equivalent circuit when only v_{cvtc} exists.

where $\boldsymbol{Y}$ is the bus admittance matrix and its value is:

$$\boldsymbol{Y}=\begin{bmatrix} Y_{Lc}+\left(0.5Y_{Lg}+Y_{Cf}\right)+Y_{Cf} & -\left(0.5Y_{Lg}+Y_{Cf}\right) & -Y_{Cf} \\ -\left(0.5Y_{Lg}+Y_{Cf}\right) & Y_{Lc}+Y_{Cf}+\left(0.5Y_{Lg}+Y_{Cf}\right) & -Y_{Cf} \\ -Y_{Cf} & -Y_{Cf} & Y_{Lc}+Y_{Cf}+Y_{Cf} \end{bmatrix}$$

where Y_{Lg}, Y_{Lc}, and Y_{Cf} are the admittance of L_g, L_c, and C_f respectively.

Because $I_g = \left(V_1 - V_2\right)/\left(2sL_g\right)$, I_g can be derived in the matrix format as:

$$I_g=\frac{1}{2sL_g}\begin{bmatrix}1 & -1 & 0\end{bmatrix}\begin{bmatrix}V_1\\V_2\\V_3\end{bmatrix}=\frac{1}{2sL_g}\begin{bmatrix}1 & -1 & 0\end{bmatrix}\boldsymbol{Y}^{-1}Y_{Lc}\begin{bmatrix}V_1\\V_2\\V_3\end{bmatrix}, \text{ and}$$

can be simplified as:

$$I_g=\frac{V_{cvta}-V_{cvtb}}{s^3L_gL_c\left(3C_f\right)+s\left(L_g+L_c\right)} \tag{37}$$

Because the most significant harmonic is V_{har}, and $V_{cvta} \leq V_{har}$, $V_{cvtb} \leq V_{har}$. The maximum value of I_g is as (38),

$$I_{g-har} \leq \frac{2V_{har}}{s^3L_gL_c\left(3C_f\right)+s\left(L_g+L_c\right)} \tag{38}$$

Define $G_{LCL\text{-}har}$ as the maximum harmonic transfer function, then,

$$G_{LCL-har}=\frac{I_{g-har}}{V_{cvt-har}}=\frac{2}{s^3L_gL_c\left(3C_f\right)+s\left(L_g+L_c\right)} \tag{39}$$

With a balanced 3-ϕ system, the transfer function of the *LCL* filter is $G_{LCL-har}=\dfrac{1}{s^3L_gL_c\left(3C_f\right)+s\left(L_g+L_c\right)}$, and the maximum voltage harmonic remains unchanged as (26). Therefore, the worst scenario for I_g harmonics happens when connected to a 1-ϕ grid, and the LCL filter designed for the proposed 1-ϕ system can meet the grid current harmonic for the balanced 3-ϕ system.

Eq. (37) shows that V_{cvtc} has no contribution to I_g. To analyse the reason, the superposition theory is applied. Thus, all the voltage sources except V_{cvtc} are shorted as shown in Fig. 27. It is seen that *Node 1* and *Node 2* are in the equal voltage potential points of a balanced Wheatstone bridge when the only v_{cvtc} is applied. Therefore, I_g is independent of V_{cvtc}.

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