Split Parallel Semi-Bridge Switching Cells for Full-Power-Range Efficiency Improvement

Yunlei Jiang, *Student Member, IEEE,* Yanfeng Shen, *Member, IEEE,* Luke Shillaber, *Student Member, IEEE,* Chaoqiang Jiang, *Member, IEEE,* and Teng Long, *Member, IEEE*

Abstract—**This paper proposes a positively-coupled-inductor (PCI) based paralleling scheme for basic semi-bridge switching cells which are formed by power MOSFETs and diodes. Both the semi-bridge switching cells and the inductors are split into two parallel parts, and thus, a small differential-mode inductance is formed between the midpoints of the parallel semi-bridge switching cells. A time-delay-based modulation strategy is applied to generate a controllable circulating current which enables all active switches to achieve the zero-current switching (ZCS) or zero-voltage switching (ZVS), and all diodes to achieve ZCS turn-off. Accordingly, the switching loss and the reverse-recovery loss can be significantly reduced. The operating principle of the proposed paralleling scheme is characterized by two complementary operation modes: desynchronized mode with soft-switching (lower switching loss) and synchronized mode with lower conduction loss. Compared with conventional soft-switching schemes, this solution features zero auxiliary switches, constant switching frequency, and improved full-power-range efficiency enabled by the dual operation modes. Furthermore, design guidelines of the PCI are presented where a novel winding arrangement is proposed and verified to obtain a controllable differential mode (DM) inductance. The operation principles and advantages of the proposed paralleling structure are comprehensively validated on both Buck and Boost dc-dc converters with Si/SiC power MOSFETs and diodes.**

Index Terms—**Parallel MOSFETs, zero-voltage switching (ZVS), zero-current switching (ZCS), dual operation modes.**

I. INTRODUCTION

THE requirements for high efficiency over full operation range have become stricter in applications such as electric vehicles [1], wind power generation [2], more electric aircraft, etc. In the search for new approaches, the adoption of switching building blocks formed by an active switch and diode pair is an industry preferred solution and lies as the foundation of classical topologies like Buck dc-dc, Boost dc-dc, and bridgeless PFC converters [3]. However, the limitation on the current ratings of power MOSFET and diode and the necessity to implement them in medium or high-power applications makes paralleling technique, both on die level and device level, an appealing choice. Generally, paralleling power devices with current sharing, as shown in Fig. 1(a), could be of advantages than employing a single high-current one in

consideration of device cost, limitation in the active area of the chip [4], and thermal stress due to limited cooling surface area [5] and is therefore considered as an inevitable approach to elevate the current capacity of the converter.

Static and transient current imbalance among parallel switching cells, as shown in Fig. 1(b), is targeted as the main issue that degrades current sharing performance and usable current rating and is therefore systematically analyzed and addressed in [6], [7] by introducing a differential choke or altering gate voltage dynamically [8] to suppress threshold voltage difference and other parameter mismatches. The second problem region of paralleling switching cells, which is specifically targeted in this paper, is about the accompanying efficiency penalty as the equivalent junction capacitance of parallel devices is significantly increased. The more devices in parallel, the larger the junction capacitance and the associated capacitance-related power losses. Particularly, in partial-load operation, the switching loss is dominated by junction capacitance-related power loss as stated in [9]. Besides, reverse recovery loss still exists for minority carrier devices, Si MOSFETs, Si IGBT, and diodes specifically, in a hard-switching scenario which results in increased power dissipation and worse electromagnetic interference (EMI) performance. On the other hand, the light-load operation typically represents the dominant use in various applications, e.g., microprocessors, EVs, and PVs [10]. The adoption of wide bandgap (WBG) devices and associated fast switching techniques [11] helps to reduce the overlapping loss and the reverse recovery loss, but the junction capacitance loss still tends to be fairly hard to address. In these regards, the light-load efficiency of the parallel switching cells is quite limited and it becomes necessary to improve the full-range efficiency at a lower cost.

To address the issues above, soft-switching could be a promising solution and numerous techniques have been proposed [12]–[14]. The soft-switching can be achieved by substituting continuous current mode (CCM) operation with other alternatives or using auxiliary devices, in the scenario where the resonant load is not obtainable. For a half-bridge (HB) switching cell, triangular current mode (TCM) [15] has been widely studied which enables soft-switching by creating a negative inductor current discharging the device junction capacitance to facilitate zero voltage switching (ZVS) before a switching ON event. It should be noted that the TCM is not fully applicable on semi-bridge switching cell due to inductor current unipolarity. Another alternative is the discontinuous current mode (DCM) [16] [17] in which the inductor current is zero for a portion of the switching cycle

and zero current switching (ZCS) is naturally achieved. Both DCM and TCM operations are featured by low switching loss, high current ripple, and variable switching frequency in many cases, which makes it a popular solution for high-frequency but low-power applications like point-of-load converters [18] and micro-inverters [19]. One method to ensure both soft-switching and CCM operation is adding auxiliary resonant circuits to the DC [20] [21] or AC [22] side of the converter, and the latter solution is widely referred to as the auxiliary resonant commutated pole (ARCP) family [22]–[25], which was first proposed by De Doncker [24]. It is stated in literature [25] that ARCP can reduce the switching loss by a factor of eight despite that auxiliary switches, which are not lossless, and inductors are necessary.

Although soft switching can be achieved with the afore-mentioned methods, CCM operation, constant switching frequency, and zero auxiliary switches can hardly be achieved simultaneously. For a semi-bridge switching cell, another basic switching unit for Buck/Boost converter, the soft-switching solutions are more limited due to current unipolarity. Apart from the solutions mentioned, adopting auxiliary switches [26], [27] among interleaved cells has been adopted. However, auxiliary switches are still required and application generality is compromised as they are only applicable to interleaving converters.

In [28], a soft-switching solution named quadrilateral current mode (QCM) operation based on paralleling HBs is proposed which can achieve all the mentioned merits simultaneously in partial load conditions by utilizing a circulating current between parallel HBs. However, the QCM solution is not validated for semi-bridge switching cells and dedicated ZVS inductors are required in [28], which increases the complexity and downgrades the power density. Aiming at overcoming the aforementioned issues and to improve the partial-load efficiency of semi-bridge switching cells, a desynchronized parallel scheme, which employs gate signals of the same switching frequency but with different turn ON/OFF delays, is proposed in this article in which (i) two or more paralleling switching cells are split into two groups which are driven independently and (ii) the split outputs of the 2 groups are closely positively-coupled in the output inductor; (iii) a differential mode inductance is established between the switch nodes of the two groups and (iv) a desynchronized modulation scheme is applied to intentionally create current imbalance for the soft-switching purpose, which significantly reduces the switching loss at partial loads. At heavy loads, the parallel semi-bridge cells are synchronized to act as one switching unit. When operating at partial loads, the proposed scheme will be engaged to desynchronize paralleled cells to realize soft switching for minimizing switching losses which are more significant at partial loads. Mode changing between synchronized and desynchronized can be seamlessly achieved. Neither additional power nor passive components are required in the proposed method for paralleled semi-bridge cells.

Compared with existing soft-switching methods, the proposed switching block based on the new paralleling scheme offers the following advantages:

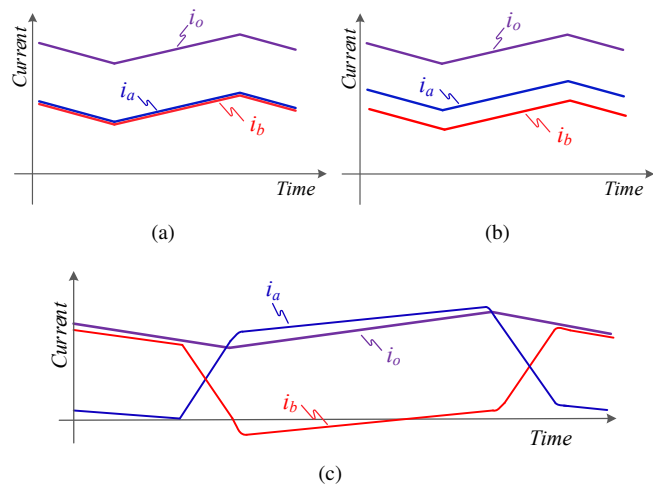- *Two operation modes enabled:* Two complementary op-

Fig. 1. Current waveforms of parallel semi-bridges under (a) ideal conditions with current sharing, (b) nonideal conditions with imbalance current due to circuit parameter mismatch, and (c) in the proposed power block which intentionally enlarges current imbalance for soft-switching purpose.

erations with completely different loss characteristics are available and the block can switch seamlessly between them for optimal efficiency performance. Specifically, soft switching is adopted at partial loads while hard switching is chosen at heavy loads.

- *Inductor current in CCM:* The output is always in CCM in two complementary operations so lower filter capacitance is required;
- *Constant switching frequency:* can be obtained in both two operations which facilities the design of EMI filter and filter inductor;
- *No Auxiliary switches or diodes added:* The switches are rated for full load condition so all the devices are indispensable at full load condition;

The remainder of this article is organized as follows. Section II and III present the derivation and operation principle of the proposed block composed of parallel semi-bridge switching cells. The design of magnetic integration is given in Section IV and Section V demonstrates the experimental results. Extension of the proposed scheme to multiple cells in parallel and systematic comparison among various soft-switching solutions are presented in Section VI. Finally, conclusions are drawn in Section VII.

II. DERIVATION OF THE PROPOSED PARALLEL SEMI-BRIDGE STRUCTURE

A. Power Loss Characteristics of SiC Power Devices in Parallel

The accumulative energy loss for a semi-bridge switching cell operating in hard switching over one switching cycle can be decomposed into conduction loss and switching loss.

From energy loss point of view, the composition of turn-on energy E_{on} and turn-off energy E_{off} of MOSFETs has been investigated extensively [29]. It is found that E_{on} loss contains an inherent portion due to the self-discharging/charging of upper-side and low-side device junction capacitance. This

portion is also referred as junction capacitance loss in this article. In a buck-type semi-bridge, the equation to calculate the junction capacitance loss E_{oss} of the high-side MOSFET and junction capacitance loss E_d of the low-side diode in a turn-on event can be derived as below,

$$E_{oss} = \int_0^{V_{dc}} v_{ds} C_{oss}(v_{ds}) \, dv_{ds} \tag{1}$$

$$E_d = \int_0^{V_{dc}} (V_{in} - v_R) C_d(v_R) \, dv_R \tag{2}$$

where C_{oss} is the miller capacitance of the high-side MOSFET and C_d is the junction capacitance of the low-side diode. v_R and v_{ds} denote the reverse voltage across the diode and drain-source voltage of the MOSFET, respectively. From equation (1) and (2), the E_{oss} and E_d losses are constant and independent of junction temperature and the device current [30], if the operating voltage for the SiC MOSFET is fixed. Besides, paralleling more devices is expected to multiple the equivalent junction capacitance.

At different duty ratios and output currents, the calculated power losses of parallel semi-bridge switching cells are illustrated in Fig. 2.
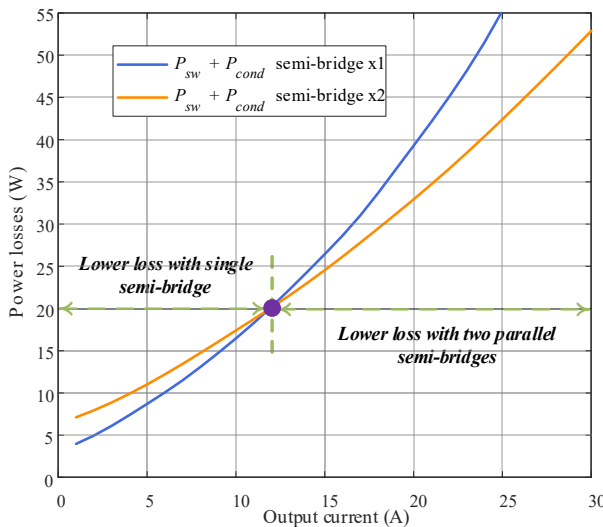

Fig. 2. Conduction and switching losses of different numbers of parallel semi-bridges operating in CCM and at a switching frequency of 200 kHz. Each switching cell is composed of one IMZA65R048M1H SiC MOSFET (650 V, 48 mΩ) from Infineon and one CVFD20065A Schottky diode (650V) from Cree.

As can be observed from Fig. 2, paralleling more devices causes reduced efficiency at partial loads due to the existence of larger equivalent junction capacitance. Thus, for the same device, a single semi-bridge switching cell has the lowest loss from 0 to 16A. As the load raises, the conduction loss increases, and eventually, the single semi-bridge generates higher power loss than two or more parallel semi-bridges. Although paralleling more semi-bridges yields a much smaller conduction loss at high output current, light-load efficiency is significantly compromised. In these regards, the light load and heavy load efficiencies appear to conflict with each other in a hard-switching scenario. In the scheme, soft-switching can be achieved for parallel semi-bridges at light load so it appears to

be a "single" semi-bridge from the viewpoint of power loss. Meanwhile, high efficiency resulting from low conduction loss at high load is not lost.

B. General Soft-switching Conditions for Sem-bridge Switching Cell

For soft-switching operation, it is crucial to specify the conditions for ZVS and ZCS. ZVS turn-on requires a current to charges or discharges the output capacitance of the switching device before the device is gated ON. For example, in a Buck-type semi-bridge, ZVS turn-ON could be achieved if a negative inductor current appears prior to the gating ON event of the device. For a single switching cell, the condition is met by applying the TCM strategy. For the proposed power block composed of parallel semi-bridges, the condition is met by allocating the current internally between parallel devices which will be discussed in the next section.

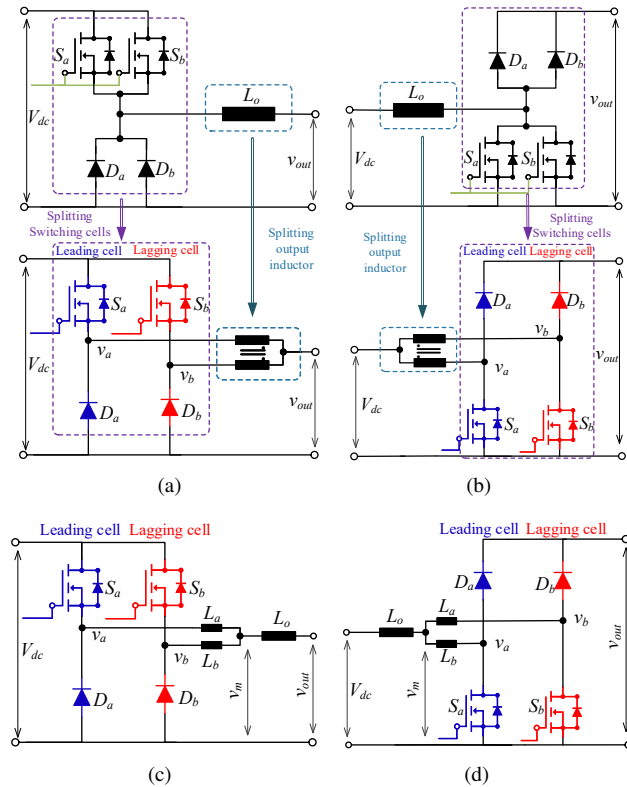### C. The Proposed Split Parallel Semi-Bridge Switching Cells

Fig. 3. Configuration of the paralleling scheme (a) Buck-type configuration, (b) Boost-type configuration and corresponding equivalent circuits ((c) and (d)).

Fig. 3 shows the configuration of the split parallel semi-bridge switching cells. The scheme is composed of two parallel switching cells S_a-D_a and S_b-D_b. S_a and S_b denote power MOSFETs and D_a and D_b represent power diodes. The switching nodes of two parallel cells are split, as shown in Fig. 3(a) and (b), and a positively-coupled-inductor (PCI) is used in replace of the filter inductor L_o. According to the general model of the coupled inductor, differential mode

(DM) inductors L_a and L_b are expected to appear between the midpoints (v_a and v_b) of two legs. Thus, the integrated PCI provides both DM and common-mode (CM) inductance for facilitating soft-switching and filtering, respectively. Buck-type semi-bridge (Fig. 3(a)) and Boost-type semi-bridge (Fig. 3(b)) are adopted depending on different operation requirements and will be analyzed separately in the following sections.

In the corresponding equivalent circuits as shown in Fig. 3(c) and (d), V_{dc} refers to the input voltage, v_{out} refers to the load voltage and v_m denotes the common output voltage. The parallel semi-bridge switching cells are divided into two groups: the leading switching cell $S_a - D_a$ and the lagging switching cell $S_b - D_b$. The gates of S_a and S_b are driven independently. It is worth noting that the integration of DM and CM inductors is realized by applying a positively-coupled-inductor and the integration mechanism is introduced in the next subsection.

D. Magnetic Integration Using a Coupled Inductor for the Parallel Switching Cells
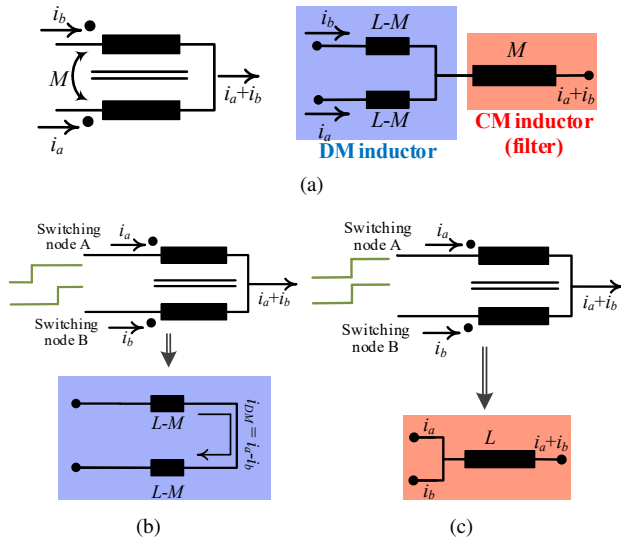

Fig. 4. General circuit model of the coupling inductor (a) and (b) DM inductance used in desynchronized mode and (c) CM inductance used in synchronization mode.

According to the practical transformer model as shown in Fig. 4 (a) [31], the core permeability is finite so the flux is not fully confined in the core, and this uncoupled flux cause leakage inductance. In the split semi-bridge switching cells, DM leakage inductance of the PCI is expected to be several μH and CM inductance (used as a filter) is the self-inductance at several hundred μH.

This integrated magnetic component has been frequently applied in resonant converters [32] and dual active bridge converters. Concerning the parallel semi-bridge configuration mentioned above, it becomes feasible to apply the leakage inductance of a positively-coupled transformer as the DM inductance (see Fig. 4(b)) and the mutual inductor as a filter (see Fig. 4(c)). The coupled inductor can be represented by an equivalent circuit with three uncoupled inductors as illustrated in Fig. 4. In the equivalent circuit, M is referred to as the

mutual inductance between winding A and winding B, and L_σ is the self-inductance of each single winding, which equals the difference between L and M, represents the leakage inductance.

III. OPERATION PRINCIPLE AND SWITCHING PATTERN OF THE PROPOSED SPLIT PARALLEL SEMI-BRIDGE CELL

A. Operation Principle

● Desynchronized mode for light/partial loads: as shown in Fig. 5, S_a is turned on prior to S_b and turned off subsequent to S_b. The time difference between the turn-on edges is termed as ϕ_{on} while that between the turn-off edges of is termed as ϕ_{off}. As a result of the desynchronized gate signals, the switching-node voltages of the paralleled switching cells v_a and v_b are asynchronous as well. Moreover, the values of DM inductors L_a and L_a are considered to be identical but much smaller than that of CM inductor L_o. In this context, the CM output voltage of the paralleled switching cell is obtained as,

$$v_m(t) = \frac{v_a(t) + v_b(t)}{2} \qquad (3)$$

For the desynchronized switching pattern, v_m is a three-level waveform (0, $V_{dc}/2$, V_{dc}) since L_a and L_b operate as a voltage divider. The voltage difference between switching node voltages v_a and v_b, which is termed as DM voltage v_{ab}, establishs a circulating current i_{dm} flowing through L_a and L_b. Similar to the CM voltage, the expression of DM voltage v_{ab} and current i_{DM} can be expressed as:

$$\begin{cases} i_{DM}(t) = \frac{i_{L_a}(t) - i_{L_b}(t)}{2} \\ (L_a + L_b)\frac{di_{DM}(t)}{dt} = v_{ab}(t) \end{cases} \qquad (4)$$

The DM commutation inductors L_a and L_b are assumed to be identical (i.e., $L_a = L_b = L_c$) due to the symmetric winding structure of PCI. According to (4), i_{dm} is directly regulated by v_{ab}. Furthermore, the analytical relationship between v_m and v_{out} can be derived as,

$$\begin{cases} L_o\frac{di_{L_o}(t)}{dt} = v_m(t) - v_{out} \\ i_o(t) = i_{L_a}(t) + i_{L_b}(t) \end{cases} \qquad (5)$$

where i_o denotes the output current. Reorganizing (5) gives the expression of i_{La} and i_{Lb} in the form of CM, i.e. $i_o/2$, and DM current, respectively,

$$\begin{cases} i_{L_a}(t) = \frac{i_o(t)}{2} + i_{DM}(t) \\ i_{L_b}(t) = \frac{i_o(t)}{2} - i_{DM}(t) \end{cases} \qquad (6)$$

Equation (6) implies the possibility of shaping both i_{La} and i_{Lb} by i_{dm}, i.e. increasing or decreasing the amplitude of i_{dm} for optimizing current in power electronic devices to achieve soft-switching.

● Synchronized mode for heavy load: as shown in Fig. 5(b), the gate signals v_{gsa} and v_{gsb} are synchronized. In that case, two paralleled switching cells should operate with identical current and voltage transients so the load current is equally shared if the circuit parameters are symmetrical. In contrast with the direct paralleling counterpart, another benefit of the structure is that the current transient imbalance due to mismatches of the transistors can be well suppressed due to the existence of the DM inductor [4] [6].
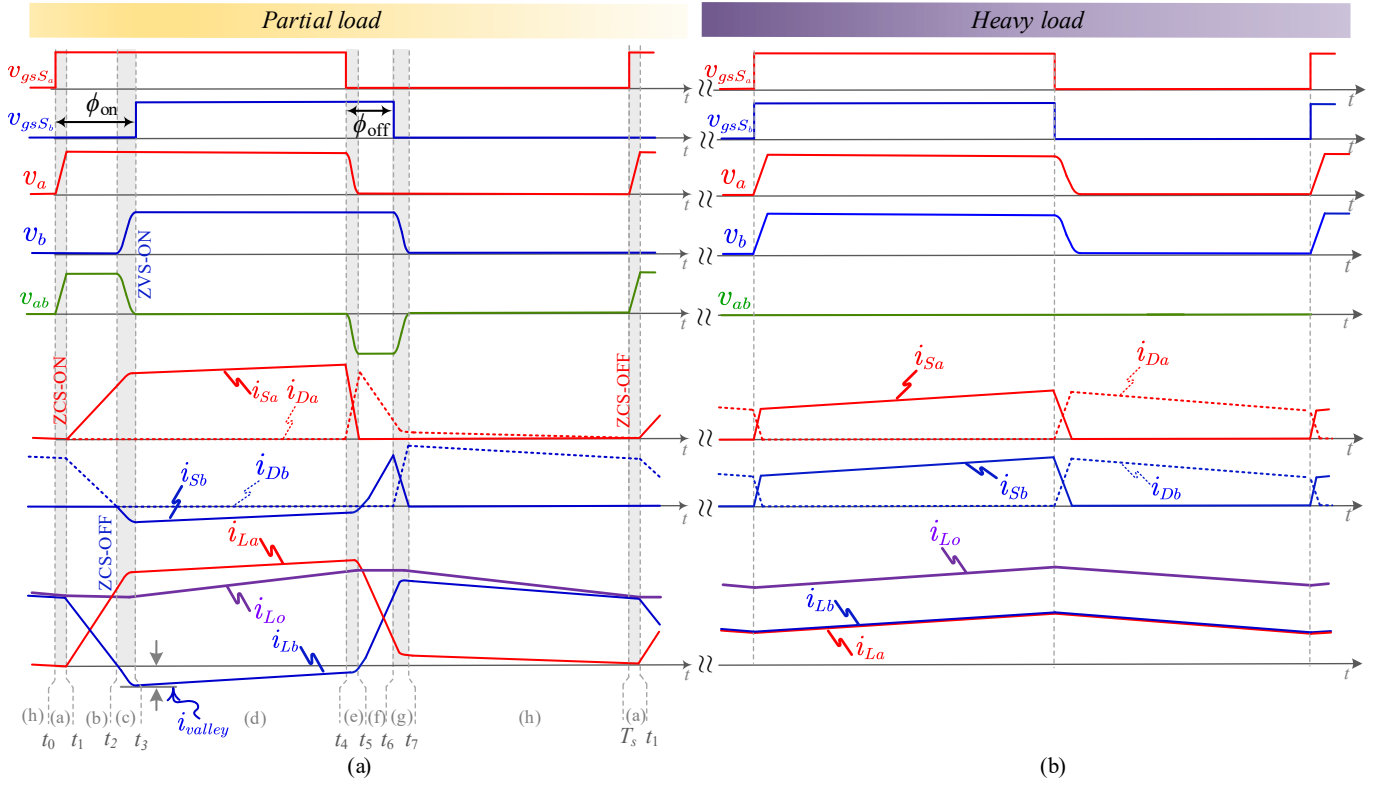
Fig. 5. Typical operation waveforms of the paralleled semi-bridge switching cells at both (a) desynchronized mode for light/partial load and (b) synchronization mode for heavy load conditions.

B. Analysis of Operation Intervals in Desynchronized Mode

The non-synchronous Buck converter (see Fig. 3(a)) is used as an example to illustrate the operating principle. The desynchronized modulation scheme is shown in Fig. 5(a).

There are total 8 intervals (a to h) within one switching cycle, among which 5 are linear intervals and 3 are resonant intervals. In linear intervals, the MOSFETs are fully turned ON or OFF with constant or infinite channel resistance $R_{ds,on}$. In resonant intervals, the circuit is dominated by resonance formed by output capacitances of MOSFETs and diodes, the DM inductors (L_a and L_b), and the CM inductor L_o. The equivalent circuits in each interval are depicted in Fig. 6. For simplifying the analysis, the diodes are assumed to be Schottky diodes without reverse recovery charge.

● t_0: Before interval (a), the current flows through the diodes of the semi-bridges D_a and D_b, and negative/zero voltage is applied to the MOSFETs: S_a and S_b.

● Interval(a) [$t_0 \sim t_1$]: Non-resonant interval, S_a ZCS turn on.

During interval (a), the internal channel of S_a is turned on after v_{gsa} reaches the threshold voltage V_{th}. Junction capacitors of S_a and D_a are discharged and charged, respectively. Meanwhile, current i_a is commuted from D_a to S_a. Before the end of the interval (a) t_1, the channel of S_a has been fully turned on with ZCS and therefore zero overlapping loss occurs. The duration of interval (a) is negligibly small considering the fast turn-on speed of MOSFET.

● Interval(b) [$t_1 \sim t_2$]: Non-resonant interval, positive DM voltage v_{ab} is established.

From t_1, D_b is conducting so a positive DM voltage v_{ab} is

established between two switching nodes, which drives DM current i_{dm} to increase linearly at the opposite direction of i_{Lb} thus i_b is decreasing linearly. i_{Lb} is expected to change polarity and becomes negative by the end of the interval (b). Current and voltage in this interval are defined by the following equations

$$
\begin{cases}
i_{CM}(t) = I_{CM,0} + \frac{1-2D}{4L_o}V_{dc}(t-t_1) \\
i_{DM}(t) = I_{DM,0} + \frac{V_{dc}}{2L_c}(t-t_1) \\
i_{La}(t) = i_{CM}(t) + i_{DM}(t), i_{Lb}(t) = i_{CM}(t) - i_{DM}(t) \\
v_{ab} = v_{DM} = V_{dc} - R_{ds,on}i_{La} + V_F \approx V_{in}
\end{cases}
\tag{7}
$$

where V_F is the forward voltage of the diode and D is the duty ratio of the circuit. The duration of this interval is denoted as t_{12}.

● Interval(c) [$t_2 \sim t_3$]: Resonant interval 1:

In this interval, MOSFET output capacitor C_{ossb} of S_b and diode junction capacitor C_{Db} of D_b form the resonant circuit with L_a and L_b. C_{ossb} is discharged from V_{dc} to 0V while C_{Db} is charged from 0 to the positive rail of V_{dc}. It should be noted that $C_{ossa} = C_{ossb} = C_{oss}$ and $C_{Da} = C_{Db} = C_D$ since identical devices are used for parallel semi-bridges. Besides, the valley current of i_{Lb} is dependent on the differential mode inductance and junction capacitance. The resonant transition can be described with the trajectory depicted in the state-plane in Fig. 8. The center of the trajectory circle locates at (V_{dc}, 0), which is the steady-state locus. Time-domain behavior of the second-order resonant circuit in this interval can be described by:

$$\begin{cases} i_{La}(t) = I_{L_o,t_2} + \frac{V_{dc}}{Z_r}\sin[\omega_r(t-t_2)] \\ i_{Lb}(t) = -\frac{V_{dc}}{Z_r}\sin[\omega_r(t-t_2)] \\ v_a(t) = V_{dc} \\ v_b(t) = V_{dc}\{1 - \cos[\omega_r(t-t_2)]\} \end{cases} \quad (8)$$

where $Z_r = \sqrt{2L_c/(C_{oss}+C_D)}$ is the characteristic impedance of the $L-C$ circuit and ω_r, which is detailedly expressed in equ. (17), is the resonant angular frequency.

According to equation (8), it is found that switch-node voltage v_b will discharge to 0 by the end of this interval, indicating that S_b can be subsequently turned on with ZVS in the next interval (d). The duration of his interval is denoted as t_{23} and can be calculated from the trajectory presented in subsection C.
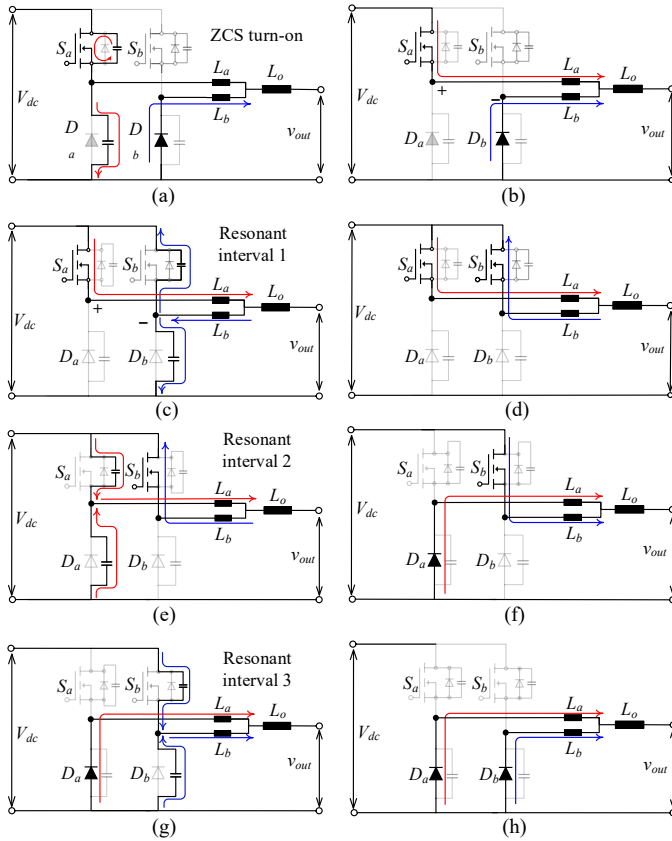

Fig. 6. Operating intervals of parallel buck-type semi-bridges within one switching cycle, among which 3 are resonant intervals and 5 are linear intervals. (a) $[t_0 \sim t_1]$. (b) $[t_1 \sim t_2]$. (c) $[t_2 \sim t_3]$. (d) $[t_3 \sim t_4]$. (e) $[t_4 \sim t_5]$. (f) $[t_5 \sim t_6]$. (g) $[t_6 \sim t_7]$. (h) $[t_7 \sim T_s]$.

• Interval(d) $[t_3 \sim t_4]$: S_b ZVS turn-on, high-side MOSFETs are conducting.

S_b is turned on with ZVS at t_3 when the voltage across S_b is zero. Then, the differential voltage v_{ab} is dominated by the difference between voltage drops on S_a and S_b,

$$\begin{cases} 2L_o\frac{di_{CM}(t)}{dt} = (1-D)V_{dc} - R_{ds,on}i_{CM}(t) \\ L_c\frac{di_{DM}(t)}{dt} = -R_{ds,on}i_{DM}(t) \end{cases} \quad (9)$$

Solving equation (9) yields

$$\begin{cases} i_{CM}(t) = \frac{(1-D)V_{dc}}{R_{ds,on}} + \left(I_{CM,t3} - \frac{(1-D)V_{dc}}{R_{ds,on}}\right)e^{-\frac{R_{ds,on}}{2L_o}(t-t3)} \\ i_{DM}(t) = I_{DM,t3}e^{-\frac{R_{ds,on}}{L_c}(t-t3)} \\ i_{La}(t) = i_{CM}(t) + i_{DM}(t), i_{Lb}(t) = i_{CM}(t) - i_{DM}(t) \end{cases} \quad (10)$$

In this interval, i_{DM} is an exponential function of time, appearing like a rising negative current. This interval ends at $t = t_4$, when zero/negative gate voltage is applied on S_a.

• Interval(e) $[t_4 \sim t_5]$: Resonant interval 2:

At the beginning of the interval (e), S_a is given low gate signal and its internal channel is, therefore, turned off. Output capacitor of S_a is charged from zero to V_{dc} and output capacitor of D_a is discharged from V_{dc} to zero via the resonance circuit formed with L_a, L_b and the process is regulated by the equation:

$$\begin{cases} i_{La}(t) = I_{L_a,t_4}\cos[\omega_r(t-t_4)] \\ i_{Lb}(t) = I_{L_o,t_4} - I_{L_a,t_4}\cos[\omega_r(t-t_4)] \\ v_a(t) = V_{dc} - Z_r I_{L_a,t_4}\sin[\omega_r(t-t_4)] \\ v_b(t) = V_{dc} \end{cases} \quad (11)$$

where I_{L_a,t_4} denotes the current through L_a at t_4. The switching node voltage v_a is expected to drop to 0 at t_5, the end of the resonant interval.

• Interval(f) $[t_5 \sim t_6]$: Non-resonant interval, negative DM voltage v_{ab} is established.

After t_5, D_a conducts and a negative DM voltage is established between two switching nodes. i_{La} begins to decrease and i_{Lb} begins to increase. This interval ends when i_{La} is small enough so ZCS turn-ON could be achieved after interval (g). The inductor currents and the differential voltage can be depicted as,

$$\begin{cases} i_{CM}(t) = I_{CM,t5} + \frac{1-2D}{4L_o}V_{dc}(t-t_5) \\ i_{DM}(t) = I_{DM,t5} - \frac{V_{dc}}{2L_c}(t-t_5) \\ i_{La}(t) = i_{CM}(t) + i_{DM}(t), i_{Lb}(t) = i_{CM}(t) - i_{DM}(t) \\ v_{ab} = v_{DM} = -V_{dc} + R_{ds,on}i_{Lb}(t) - V_F \approx -V_{dc} \end{cases} \quad (12)$$

where $I_{DM,t5}$ and $I_{CM,t5}$ denote the CM and DM currents at t_5, respectively. This interval terminates at $t = t_6$ when S_b is turned OFF.

• Interval (g) $[t_6 \sim t_7]$: Resonant interval 3

At the end of interval (e), S_b turned off. Since i_{Lb} is positive, the output capacitance of S_b is charged to the positive rail of V_{dc}, and the voltage across D_b is zero by the end of this interval.

$$\begin{cases} i_{La}(t) = I_{Lo,t6} - \\ \quad I_{La,t6}\cos[\omega_r(t-t_6)] - \frac{V_{dc}}{Z_r}\sin[\omega_r(t-t_6)] \\ i_{Lb}(t) = I_{Lb,t6}\cos[\omega_r(t-t_4)] + \frac{V_{dc}}{Z_r}\sin[\omega_r(t-t_6)] \\ v_a(t) = 0 \\ v_b(t) = V_{dc}\cos[\omega_r(t-t_6)] - Z_r I_{Lb,t6}\sin[\omega_r(t-t_6)] \end{cases} \quad (13)$$

where $I_{La,t6}$ and $I_{Lb,t6}$ denote the current through L_{La} and L_{Lb} at $t = t_6$.

- Interval (h) $[t_7 {\sim} T_s]$: Low-side diodes conducting

In interval (h), both S_a and S_b have been completely turned off so only the low-side diodes are conducting. The two switching node voltages v_a and v_b are determined by the forward voltage of two diodes. L_a and L_b keep discharging in this interval and the current through L_a is expected to reach zero by the end of this interval.

$$
\begin{cases}
i_{CM}(t) = \dfrac{-V_F - DV_{dc}}{R_D} + \left(I_{CM,t7} + \dfrac{V_F + DV_{dc}}{R_D} \right) e^{-\frac{R_D}{2L_o}(t-t_7)} \\
i_{DM}(t) = I_{DM,t7} e^{-\frac{R_D}{L_c}(t-t_7)} \\
i_{La}(t) = i_{CM}(t) + i_{DM}(t), \; i_{Lb}(t) = i_{CM}(t) - i_{DM}(t)
\end{cases}
\tag{14}
$$

where R_D denotes the forward resistance of the diodes, $I_{CM,t7}$ and $I_{DM,t7}$ denote the CM and DM currents at $t = t_7$, respectively.

C. State Plane Analysis

In subsection A, the time-domain solution of the circuit in 8 intervals is provided. A state plane analysis corresponds to the time-domain solution is given in this subsection.

1) Equivalent circuit in the resonant stages

In resonant operation interval (c), (e), and (g), a resonant network is formed by diode junction capacitor C_D, MOSFET output capacitor C_{oss} and the DM inductor. Considering $L_o \gg L_a = L_b$, the filter inductor can be regarded as a current source during the resonant transitions and therefore open-circuited in the small-signal analysis. Moreover, junction capacitance of the MOSFETs and diodes are regarded as linear using charge-equivalent values.
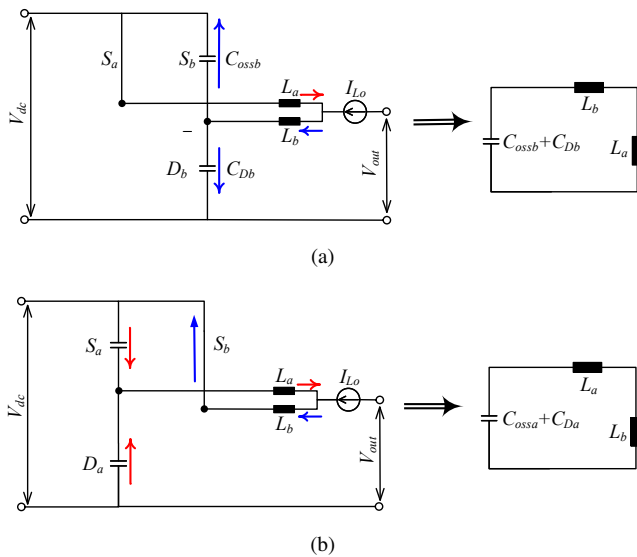

(a)

(b)

Fig. 7. Equivalent resonant circuit of the paralleling semi-bridge in (a) resonant stage 1 and 3 (b) resonant stage 2.

Based on these assumptions, the resonant network could be simplified to a second-order LC system, as shown in Fig. 7. The expression of characteristic impedance Z_r can be therefore given as,

$$
Z_r =
\begin{cases}
\sqrt{\dfrac{L_a + L_b}{C_{oss,a} + C_{D,a}}}, & \text{Resonant state 2} \\
\sqrt{\dfrac{L_a + L_b}{C_{oss,b} + C_{D,b}}}, & \text{Resonant states 1 and 3}
\end{cases}
\tag{15}
$$

Due to the nonlinearity of the output capacitance, all the output capacitance in (15) are represented by a charge-equivalent capacitance in the form of,

$$
\begin{cases}
C_{o,qe} = \dfrac{Q_{oss}}{V_{dc}} = \dfrac{1}{V_{dc}} \int_0^{V_{in}} C_{oss} \, dv_{ds} \\
C_{D,qe} = \dfrac{Q_D}{V_{dc}} = \dfrac{1}{V_{dc}} \int_0^{V_{in}} C_D \, dv_R
\end{cases}
\tag{16}
$$

where Q_{oss} and Q_D represent the total charge of the MOSFET and the diode. The accuracy of the charge-equivalent capacitance in predicting the resonant behavior has been justified in [15]. Based on that, the resonant angular frequency can be expressed as

$$
\omega_r = \frac{1}{\sqrt{(C_{o,eq} + C_{D,eq})(L_a + L_b)}}
\tag{17}
$$

2) V-I Trajectory

Further on the aforementioned derivation, the state plane diagrams depicting the trajectory of inductor current (scaled by the characteristic impedance of the resonant circuit given in equ. (15)) with respect to the drain-source voltage are demonstrated in Fig. 8.
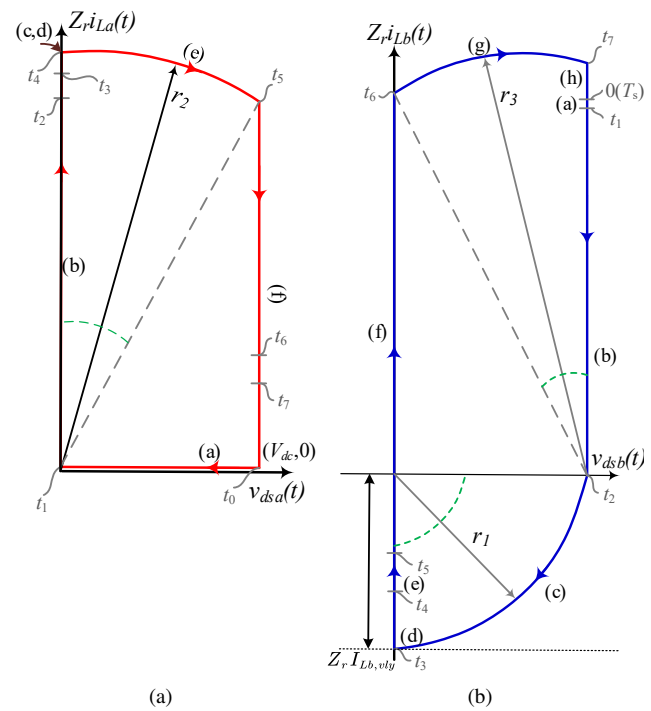

(a)

(b)

Fig. 8. State plane trajectory for the 8 operation intervals in Fig. 5, corresponding to (7) – (14). (a) $Z_r \times i_{La}$ with respect to drain-source voltage v_{dsa}. (b) $Z_r \times i_{Lb}$ with respect to drain-source voltage v_{dsb}.

From Fig. 8, the circle radius r_1 is determined by the distance between the initial and steady-state locus and is therefore calculated as $r_1 = V_{dc}$ in this case. Based on that, we have the ZVS valley current of i_{Lb} as,

$$
I_{Lb,vl} = -\frac{V_{dc}}{Z_r}
\tag{18}
$$

D. Circuit Simplification

As presented in (10) and (14), CM and DM current in non-resonant intervals are essentially the time-domain solutions of

first-order circuits, and their behaviors are largely determined by the CM time-constant $\tau_{CM} = \frac{2L_o}{R_{ds,on}}$ and the DM time-constant $\tau_{DM} = \frac{L_c}{R_{ds,on}}$. For τ_{CM}, its value is much (10 times) larger than the duration of the intervals, i.e. t_{34} and t_{67}, which indicate that τ_{CM} is large enough for its time constant to be outside the time scale of transition. Therefore, a first-order linear approximation is used to describe the behavior of $i_{CM}(t)$ in non-resonant intervals.

The value of DM inductance, on the other side, is at least one order of magnitude smaller than that of CM inductance, which indicates that $i_{DM}(t)$ decays with time exponentially in these non-resonant intervals, i.e. t_{34} and t_{67}.

(a) Commutation at $t = T_0$ and T_1

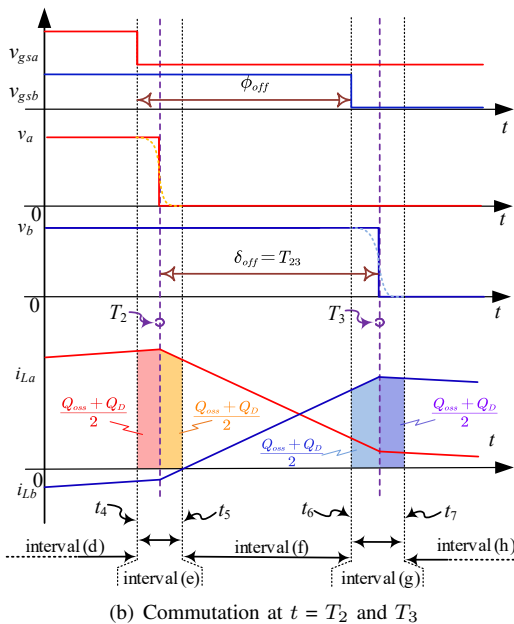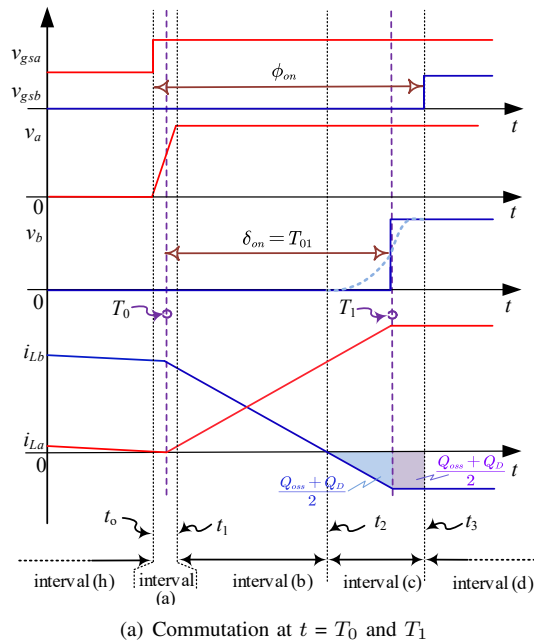(b) Commutation at $t = T_2$ and T_3

Fig. 9. Commutation waveforms using a charged-based linear MOSFET model.

For the resonant intervals, i.e. (c), (e), and (g), a charge-

based linear MOSFET model is employed to achieve an approximation of the nonlinear output capacitance of MOS-FET and diode. With this model, each resonant interval is split into two subintervals where half of the total junction charge, i.e. $(Q_{oss} + Q_D)/2$, is charged or discharged in each subinterval. The switch-node voltage jumps between V_{dc} and 0 in this model and therefore becomes a two-level waveform. The accuracy of the linear capacitor model in predicting both resonant time and the behavior of charging current has been justified in [15]. The linear charge model helps to linearize the resonant transitions without altering the during of time, thus, resonant interval (c), (e), and (g) can be merged with their adjacent non-resonant intervals (interval (c) is amalgamated with interval (b)&(d); interval (e) is amalgamated with interval (d)&(f); interval (g) is amalgamated with interval (f)&(h)).

For interval (a) where the hard-switching of S_a happens, the change of switching-node voltage v_a is assumed to be linear with rapid switching. This observation justifies dividing interval (a) into two stages merged into the interval (h) and (b), respectively. Based on the simplification of both non-resonant and resonant intervals, only four intervals, i.e. interval (b), (d), (f), and (h), are used in one switching period. For clarity, these four intervals are renamed as intervals I, II, III, and IV and are spaced apart by time instants T_1, T_2, and T_3, and T_0, T_s are the start and end of each switching period, respectively. Equations (7), (10), (12), and (14) for intervals (b), (d), (f), and (h) can be organized by following the simplification principle of linear intervals,

Interval I. $\begin{cases} i_{CM}(t) = I_{CM,0} + \frac{1-2D}{4L_o}V_{dc}(t-T_0) \\ i_{DM}(t) = I_{DM,0} + \frac{V_{dc}}{2L_c}(t-T_0) \end{cases}$

$$(19)$$

Interval II.

$$\begin{cases} i_{CM}(t) = I_{CM,T1} + \frac{R_{ds,on}}{2L_o}\left[\frac{(1-D)V_{dc}}{R_{ds,on}} - I_{CM,T1}\right](t-T_1) \\ = I_{CM,T1} + \frac{(1-D)V_{dc}}{2L_o}(t-T_1) \\ i_{DM}(t) = I_{DM,T1}e^{-\frac{R_{ds,on}}{L_c}(t-T1)} \end{cases}$$

$$(20)$$

Interval III. $\begin{cases} i_{CM}(t) = I_{CM,T2} + \frac{1-2D}{4L_o}V_{dc}(t-T_2) \\ i_{DM}(t) = I_{DM,T2} - \frac{V_{dc}}{2L_c}(t-T_2) \end{cases}$

$$(21)$$

Interval IV.

$$\begin{cases} i_{CM}(t) = I_{DM,T3} - \frac{R_D}{2L_o}\left(I_{CM,T3} + \frac{V_F+DV_{dc}}{R_D}\right)(t-T_3) \\ = I_{CM,T3} - \frac{V_F+DV_{dc}}{2L_o}(t-T_3) \\ i_{DM}(t) = I_{DM,T3}e^{-\frac{R_D}{L_c}(t-T_3)} \end{cases}$$

$$(22)$$

E. Steady-state Solution and Derivation of Time Intervals

In the steady-state, the following conditions are ought to be met. Firstly, it can be seen that the currents i_{La} at 0 and i_{Lb} at T_1 could be approximated by $I_{La,T0}$ and $I_{Lb,T2}$:

$$\begin{cases} I_{La,T0} \approx I_{La,t0} = 0 \\ I_{Lb,T1} \approx I_{Lb,t2} = -I_{Lb,vl} \end{cases} \tag{23}$$

Moreover, both i_{CM} and i_{DM} are ought to be equal at $t = T_0$ and $t = T_s$:

$$I_{CM,T0} = I_{CM,T_s} \tag{24}$$

$$I_{DM,T0} = I_{DM,T_s} \tag{25}$$

Substituting the steady-state condition (24) and (25) into (19)-(22) yields:

$$\begin{cases} I_{CM,T0} = \frac{\bar{I}_{Lo}}{2} - \frac{[\delta_{on}+(D-1)T_s]\left\{D(V_{dc}-V_F)+\left(\frac{\delta_{on}}{T_s}-1\right)V_F\right\}}{4L_o} \\ \qquad \approx \frac{\bar{I}_{Lo}}{2} - \frac{[\delta_{on}+(D-1)T_s]\{D(V_{dc}-V_F)-V_F\}}{4L_o} \\ I_{CM,T1} = \frac{\bar{I}_{Lo}}{2} - \frac{(1-D)\{-T_sV_F+\delta_{on}(V_F-V_{dc})+DT_s(V_F+V_{dc})\}}{4L_o} \end{cases} \tag{26}$$

where $\overline{I_{Lo}}$ denotes the average load current in this switching cycle. Then the initial inductor current at T_0 and T_1 can be got from (26):

$$\begin{cases} I_{La,T0} = 0, I_{Lb,T0} = 2I_{CM,T0} \\ I_{La,T1} = 2I_{CM,T1} + I_{Lb,vl}, I_{Lb,T1} = -I_{Lb,vl} \end{cases} \tag{27}$$

As aforementioned, the DM inductance is comparably low and the pulsewidths of δ_{on} and δ_{off} are much shorter compared with the switching period T_s. Therefore, the presence of these two delays has a limited influence on the output current so it is assumed initially that $\delta_{on} = \delta_{off}$. Substituting (26) and (27) into (19) gives the analytical expressions of T_{01}, i.e. δ_{on}:

$$\delta_{on} = \frac{2L_c\left[2L_o\left(\overline{I_{Lo}}-I_{Lb,vl}\right)-(1-D)\{DV_{dc}+V_F\left(D-1\right)\}T_s\right]}{2L_oV_{dc}-L_c\left\{V_{dc}+2\left(D-1\right)V_F\right\}} \tag{28}$$

Since T_{01} has been obtained, substituting (28) into (19)-(22) yields the analytical expressions of T_{23}, i.e. δ_{off}:

$$\delta_{off} = \frac{L_c}{R_D}W_o\left(A\right) + \frac{\delta_{on}V_{dc}+2I_{DM,T0}L_c}{V_{dc}}e^{\frac{R_{ds,on}(\delta_{on}-DT_s)}{L_c}} \tag{29}$$

where

$$A = \frac{-2I_{DM,T0}R_D}{V_{in}}\exp\left[R_D\frac{(1-D)T_s}{L_c}+B\right]$$

$$B = -\frac{R_D\left(2I_{DM,T0}L_c+\delta_{on}V_{dc}\right)\exp\left\{R_{ds,on}\frac{(\delta_{on}-DT_s)}{L_c}\right\}}{V_{dc}L_c}$$

, and W_0 is the zeroth branch of the Lambert W function.

As can be observed from (28) and (29), both δ_{on} and δ_{off} are functions of average load current $\overline{I_{Lo}}$, duty cycle D, and input voltage V_{dc}. In the control implementation, these variables are sampled and delay times are expected to be updated accordingly in each control cycle.

F. Determination of Switching Delays

The duration of time intervals T_{01}, i.e. δ_{on}, and T_{23}, i.e. δ_{off}, are determined by (28) and (29). Due to the existence of resonant transitions, the time delays of the rising and falling MOSFET gate signals are not equal to δ_{on} and δ_{off}, as shown in Fig. 9. The MOSFET turn-on delay ϕ_{on} is larger than δ_{on} while the turn-off delay ϕ_{off} is smaller than δ_{off}. Therefore, turn-on delay ϕ_{on} is derived as:

$$\phi_{on} = \delta_{on} + \frac{t_{HS}}{2} - \frac{Q_{oss}+Q_D}{2I_{Lb,vl}} \tag{30}$$

where t_{HS} is the ZCS turn-on time of S_a. Due to the fact that S_a is always turned on with zero current in desynchronized mode, t_{HS} is regarded as constant.

The calculation of turn-off delay time ϕ_{off} follows a similar process by solving Fig. 9(b) geometrically:

$$\begin{aligned} \phi_{off} = & \frac{Q_{oss}+Q_D}{2I_{La,T2}} - \frac{2I_{Lb,T2}L_c}{V_{dc}} \\ & + \sqrt{\left(\frac{2I_{Lb,T2}L_c}{V_{dc}}+\delta_{off}\right)^2 - \frac{2\left(Q_{oss}+Q_D\right)L_c}{V_{dc}}} \end{aligned} \tag{31}$$

The proposed desynchronized mode operation can be applied where semi-bridge switching cells are used. As for a typical Buck converter, the corresponding control implementation is given in Fig. 10. As can be seen, the main control loop is responsible for current/voltage regulation and delay time calculation block yields ϕ_{on} and ϕ_{off} according to the load condition. Since the load current may happen to be around the mode switching point, a hysteresis control strategy is implemented to increase the immunity to disturbance which may trigger undesired oscillation between two modes during the transition. The selected operation mode is then used to determine whether the time delay between PWM signals would be implemented. In the hysteresis block, a current band is created between the desynchronized and synchronized operations. In this way, the operation state transition will only be triggered when the load current is between an upper and a lower band.

IV. DESIGN OF THE INTEGRATED INDUCTOR

A. General Leakage Inductance Model

The leakage inductance of a transformer represents the magnetic field that escapes from the core and returns through the air and is determined by the configuration of winding and the dimension of the core window. If two windings are segregated as shown in Fig 11 (a), the gap between the two windings increases the leakage inductance. If turns of each winding are laid one by one in a sandwich structure as shown in Fig 11 (b), the leakage inductance will be minimized. For the parallel configuration proposed, the value of leakage inductance is closely related to the ZVS valley current, conduction loss, and the during of resonant intervals and is, therefore, should be deliberately designed to achieve optimal system efficiency.
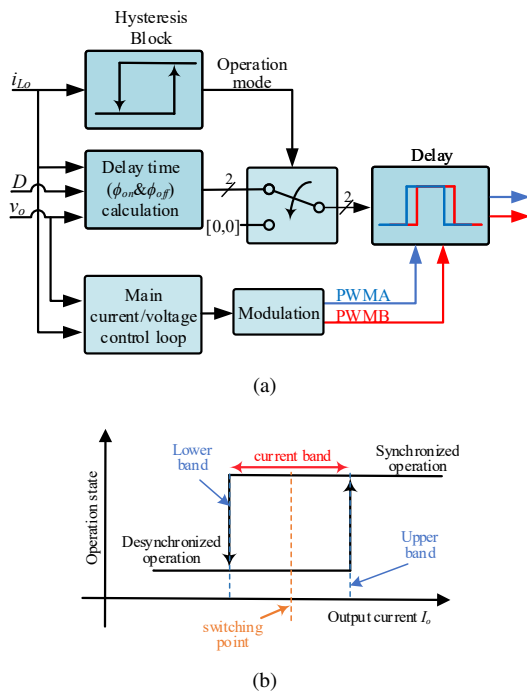
(a)

(b)

Fig. 10. Schematic diagram of the control design for the split parallel semi-bridge switching cells solution implemented in a Buck converter. (a) Block diagram of the main control loop, delay time calculation, and hysteresis mode transition. (b) Hysteresis block.
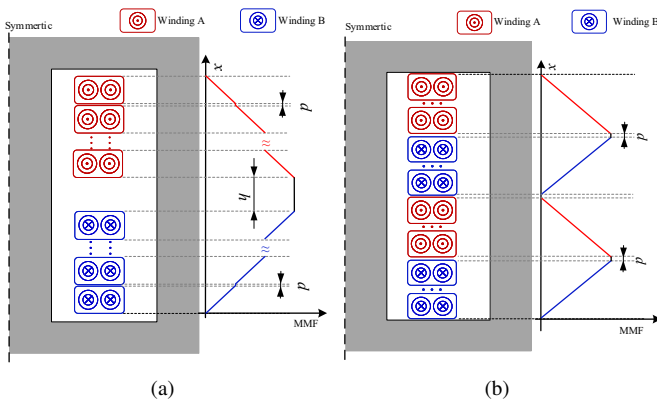

Fig. 11. Alternative winding configurations for achieving (a) higher and (b) lower leakage inductance and corresponding MMF diagrams.

B. Proposed Winding Configuration with a Controllable Leakage Inductance

In Fig. 12, a winding arrangement is proposed by dividing the winding into 3 subsectors. Sector α and γ are positioned at the sides of the core window while Sector β locates at the mid of the window. Sector β lies between Sector α and γ. In this sector, the coils of winding A and B are overlapped and therefore the MMF is expected to cancel out from the perspective of 1-D model. Such arrangement provides control over the leakage inductance in two ways:

1) Adjusting the distance between Sector α, γ, and β by increasing or decreasing h;

2) Adjusting the turn numbers in Sector α and β.
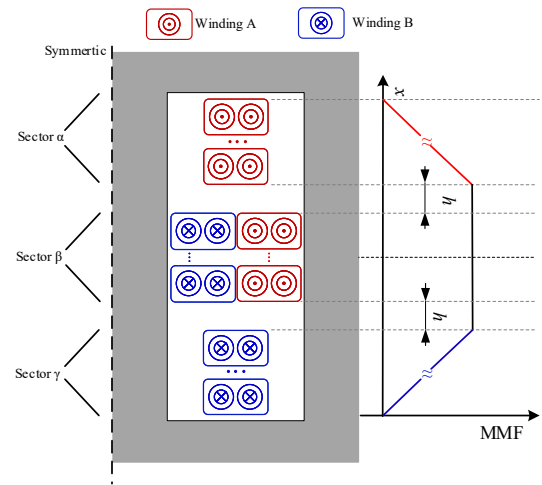

Fig. 12. Proposed winding arrangement for achieving a controllable leakage inductance.

C. Analytical Approach to Calculate the Leakage Inductance

There are two ways to calculate the leakage inductance: FEM simulation and analytical method. The analytical methods are used here to extract the leakage inductance from the coupled inductor. According to [33], a comprehensive comparison of existing analytical results including Roth's model, Rogowski's model [34] Margueron's model, MGD model, Kapp's model, and Dowell's model and 2-D model is proven to have better accuracy in calculating the leakage inductance since flux fringing is takin into consideration.

In particular, the Margueron model [35] [36] shows a good balance between accuracy and computation consumption and is applicable to insider-window (IW) and outside-window (OW) cross-sections. For simplicity, the deduction of the Margueron model and detailed calculation process are not presented here. In Fig. 13, the leakage field distribution of the proposed winding arrangement in an E71 core window is presented. The leakage energy distribution matches modeling results shown in Fig. 11 and the leakage energy density remains stable in the overlapping sector. To reduce valley current and inductor size, the final design adopts the E71 core (3C94 ferrite) and # 42 wire gauge (AWG) Litz wires (1050 strands, 14 turns). The inductor has a leakage inductance of 16.9 μH according to the Margueron model and the measured leakage inductance by impedance analyzer is 16.2 μH.

V. EXPERIMENTAL RESULTS

A. Experimental Settings

In order to validate the generality of the proposed semi-bridge scheme, the performance of the scheme is firstly implemented in a Buck and then a Boost DC-DC converter. DC-DC converter prototype is as shown in Fig. 13 (a), two types of devices, SiC devices, and Si devices, are utilized to extend the generality of the proposed parallel scheme.

For the case of SiC devices, two switching cells are paralleled and each cell is composed of one IMZA65R048M1H SiC MOSFET from Infineon and one CVFD20065A Schottky
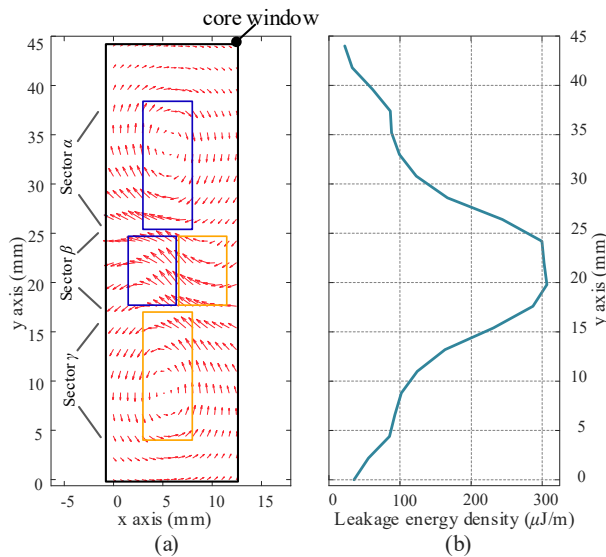
Fig. 13. Leakage field distribution within the transformer window. (a) Winding structure and magnetic field predicted by the Margueron model. (b) Leakage energy density along the y-axis in the core window.
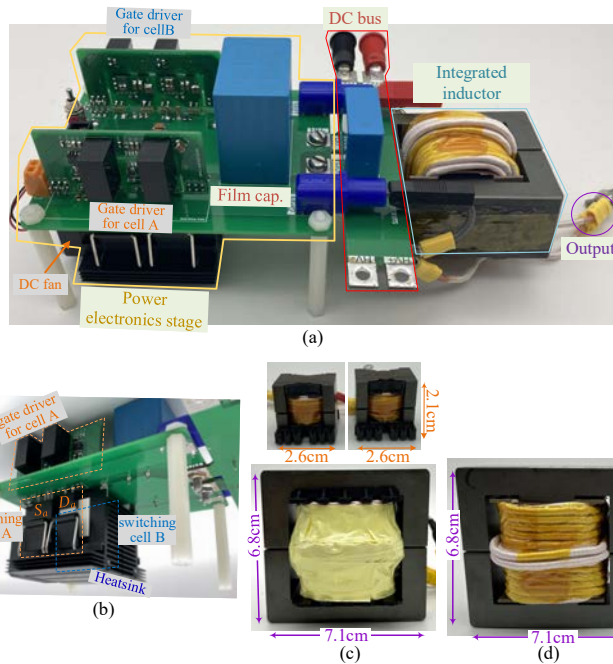

Fig. 14. Hardware prototype of the (a) proposed scheme with two switching cells in parallel, (b) power electronics stage where the heat sink is mounted on the back of the PCB, (c) fabricated discrete CM and DM inductors, and (d) fabricated integrated inductor. In the integrated magnetic design, the CM inductance is identical to the discrete CM inductance, and the DM inductance is close to two discrete DM inductance in series shown in (c).

diode from Cree, as illustrated in Fig. 14. The forced air-cooled heat sink is installed on the back of the PCB with two MOSFETs and diodes (cell A and cell B) mounted. For a fair comparison, Si counterparts with similar static characterizations, Si CoolMOS IPZ65R045C7 and Si diode IDP30E65D2 from Infineon, are chosen. Specifications of devices are given in Table I.

Detailed specifications of the magnetic design are shown in Table II. For a fair comparison, the integrated inductor utilized

TABLE I
SPECIFICATIONS OF SiC AND Si DEVICES EMPLOYED IN THE TESTS

	Devices	Parameters	Values
SiC-Based Converter Prototype	SiC MOSFET IMZA65R048M1H	$R_{ds,on}$	48 mΩ
		Q_{oss} @ 400V	29.25 nC
		Rated voltage	650 V
		Manufacturer	Infineon
	SiC Schottky diode CVFD20065A	V_F	1.35 V
		C_D @ 400V	155 pF
		Rated voltage	650 V
		Manufacturer	Cree
Si-Based Converter Prototype	Si CoolMOS IPZ65R045C7	$R_{ds,on}$	45 mΩ
		Q_{oss} @ 400V	29.13 nC
		Rated voltage	650 V
		Manufacturer	Infineon
	Si diode IDP30E65D2	V_F	1.35 V
		Q_{rr} @ 400V	0.38 μC
		Rated voltage	650 V
		Manufacturer	Infineon

the same specification as the discrete CM inductor.

TABLE II
SPECIFICATIONS OF MAGNETIC DESIGN

Specifications	Discrete DM inductor	Discrete CM inductor	Integrated CM+DM inductor
Winding Turns	6	14	14
Magnetic Core	PQ 26/20	E71	E71
Core Material	PC95 ferrite	3C94 ferrite	3C94 ferrite
Litz Wire	2 × # 42 AWG, 420 strands	# 42 AWG, 1050 strands	# 42 AWG, 1050 strands
Inductance L (μH) @ 200kHz	$5.1\mu H$	$125\mu H$	$8.1\mu H$ (DM) $125\mu H$(CM)

B. Key Operation Waveforms and State-plane Trajectory

SiC MOSFETs are used for results shown in B to F. Key operation waveforms are provided to validate the soft-switching operation, as shown in Fig. 15, and the circuit configuration is shown in Fig 3(a). In this figure, the desynchronized mode is activated and the average output current I_{Lo} is 8.2A. As shown in Fig 15, switching cell A, i.e. the leading cell, is turned on when i_{La} falls to zero while switching cell B, i.e. the lagging cell is turned on after the switch node voltage is charged to V_{dc}, corresponding to a zero voltage across the drain and source of S_b.

It is also worth noting that although the DM inductor current i_{La} and i_{Lb} are purposely controlled to reach zero or negative for soft-switching purposes, the output current i_{Lo}, i.e. sum of i_{La} and i_{Lb}, operates in CCM. All of these results match well with the theoretical analysis presented in Fig. 5.

The state-plane trajectories of the inductor currents with respect to the switch node voltage are illustrated in Fig. 16. The current/voltage waveforms are recorded and then transformed to the V-I trajectories shown in Fig. 16. The trajectories coincide well with the theoretical prediction provided in Fig. 8. The charge-based capacitance of the IMZA65R048M1H SiC MOSFET and CVFD20065A Schottky diode are 192.5 pF and 153.75 pF respectively at 400 V, which gives $Z_r = 214.9$ Ω. It is worth noting Fig. 8 is drawn with the drain-source voltage of S_a and S_b on the horizontal axis for the analysis of soft switching so Fig. 8 and Fig. 16 are actually symmetry to v = 200V vertical line.
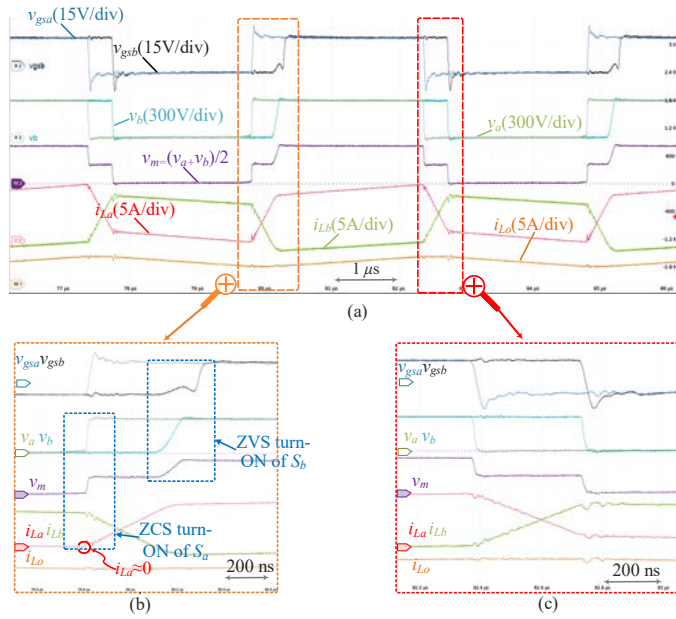
Fig. 15. Key operation waveforms of the proposed scheme based on SiC parallel semi-bridge switching cells for Buck converter when the desynchronized mode is activated. The input voltage V_{dc} = 400 V, the duty ratio D = 0.5, and switching frequency f_{sw} is 200 kHz. (a) Switch node voltages and inductor currents. Zoomed-in waveforms of (b) turn-ON and (c) turn-OFF transients of S_a and S_b.
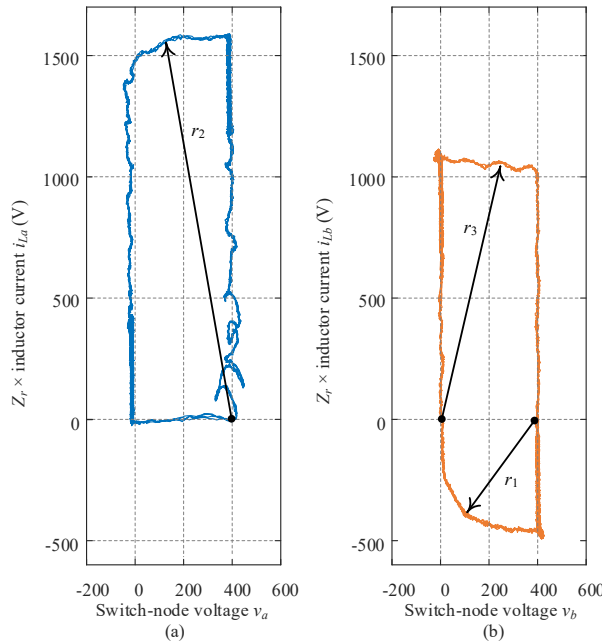

Fig. 16. State-plane trajectory of the scaled inductor current ($Z_r \times i_{La}$ & $Z_r \times i_{Lb}$) with respect to the switch-node voltage v_a & v_b for the power block. (a) $Z_r \times i_{Lb}$ with respect to v_a. (b) $Z_r \times i_{Lb}$ with respect to v_a.

C. Validation of the Magnetic Integration Design and Efficiency

In Fig. 17, an efficiency comparison is made between the discrete and integrated magnetic design with the specifications listed in Table II to validate the integrated magnetic design. It can be observed from the figure that both two designs show a similar pattern: the desynchronized mode has higher
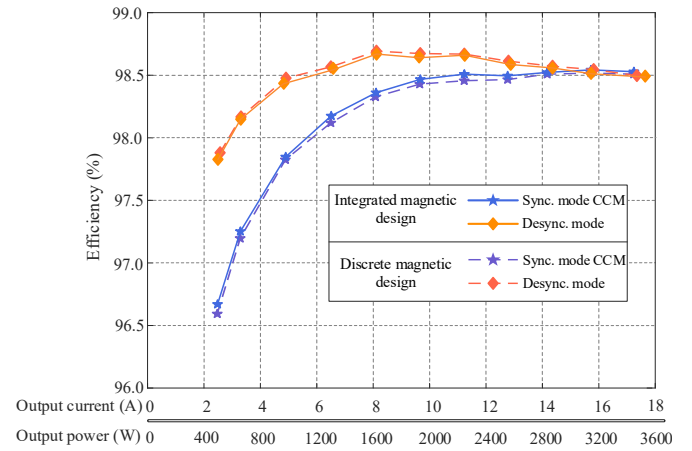

Fig. 17. Measured efficiency of the power block with the discrete and integrated inductor, respectively. The power block is configured as a Buck DC-DC converter with D = 0.5 and f_{sw} = 200 kHz. The input voltage is set as 400 V.

efficiency over synchronization mode at light load and the deviation of efficiency decreases with the increase of load current. When load current equals to 15A, the desynchronized and synchronization mode have the same efficiency.

Meanwhile, it can also be seen that integrated magnetic design owns a bit higher efficiency ($\sim$0.056%) over the discrete magnetic design in the synchronization mode and almost the same efficiency as the discrete magnetic design in the desynchronized mode. Such difference could be explained by Fig. 18 where the loss breakdown of the two magnetic designs under two operation modes is detailed.

In the loss evaluation, Dowell's model [37] is utilized to extract the winding loss of Litz wire and the improved generalized Steinmetz equation (iGSE) is used to evaluate the core loss. In Fig. 18, P_{cona} and P_{conb} denote the conduction losses of switching cells A and B. P_{on}, P_{ZCS} and P_{off} represent the hard-switching turn-on and turn-off losses of MOSFETs, respectively. As can be seen, the magnetic design doesn't make a difference in the conduction and switching loss of the devices.

However, both core loss and conduction loss of L_a and L_a are eliminated for the integrated inductor as they are physically nonexistent in the integrated magnetic design, which accounts for the loss reduction in synchronized mode. The conduction loss of the integrated magnetic design in the desynchronized mode is expected to increase as shown in Fig. 18(c), which can be explained by the difference in ac winding loss. In the desynchronized mode, more harmonics are contained in i_{La} and i_{Lb}, as they are reshaped as quadrilateral waveforms, which results in larger ac resistance and then larger winding loss. When the discrete magnetic design is applied, i_{La} and i_{Lb} flow through L_a and L_b with fewer number turns and smaller mean length per turn (56 mm) as a result of small inductance (5 μH) and core size (5.44 cm^3), so the winding loss is not significantly large (see Fig. 18 (b)). In the integrated magnetic design, however, i_{La} and i_{Lb} flow through the filter inductor itself with a larger inductance (125 μH) and also a larger core size (102 cm^3). As a result, a higher ac winding loss is expected to happen. Such loss penalty is partially compensated

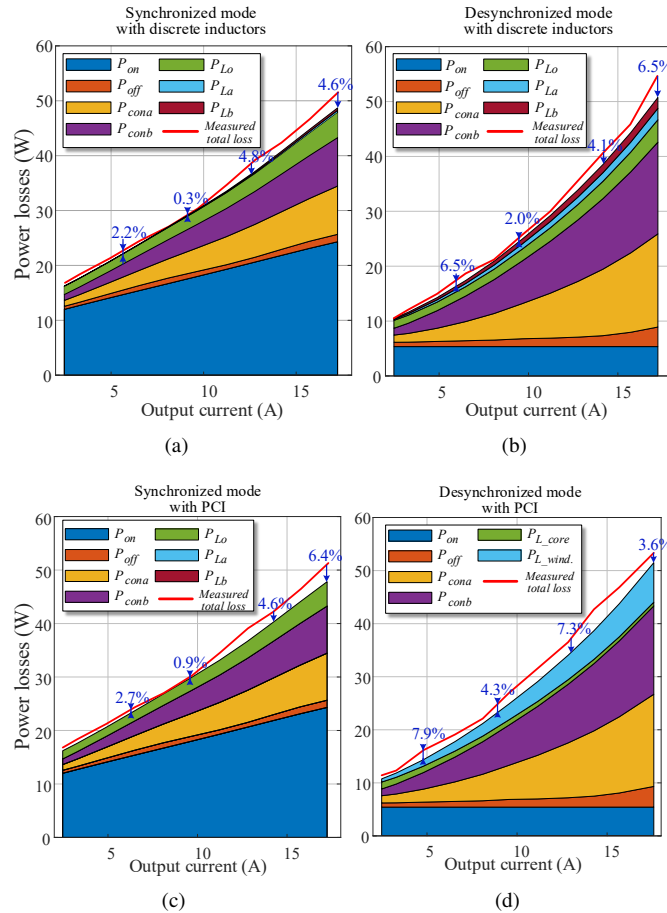by the gain bought by the elimination of two DM inductors.

Fig. 18. Comparison of power loss distribution between the discrete magnetic design and integrated magnetic design under two operation modes. Loss distribution of discrete magnetic design in (a) synchronized and (b) desynchronized mode. Loss distribution of integrated magnetic design in (c) synchronized and (d) desynchronized mode. The percentage presented represents the difference between the measured and estimated loss.

D. Efficiency Curves at Various Duty Ratios

The efficiency cures at various duty ratios are given in Fig. 19. In these tests, the integrated magnetic design is applied and the desynchronized mode obtains up to 2.38% efficiency gain when $D = 0.25$ and up to 1.2% efficiency gain when $D = 0.75$.

E. Validation of the Power Block when Configured as a Boost Converter

Application generality of the power block is further explored by configuring it as a Boost DC-DC converter and measuring efficiency curves are shown in Fig. 20. The desynchronized mode enables higher efficiency over the synchronized mode when the input current increases from 1.69A to 12.8 A. In this range, the efficiency of synchronization mode is 1.43% higher initially and then shrinks with an increased input current.

Measured current and voltage waveforms of the Boost-type block operating in the desynchronized mode are shown in Fig. 21 and the circuit configuration is shown in Fig 3(b).
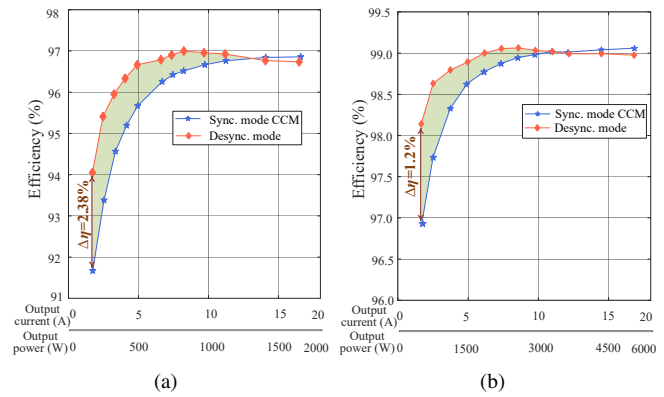

Fig. 19. Measured efficiencies of the paralleling scheme when configured as a Buck dc-dc converter with different modulation schemes: synchronous CCM and desynchronized mode and different duty ratios (a) $D = 0.25$. (b) $D = 0.75$. The input voltage $V_{dc} = 400$ V and switching frequency f_{sw} equals 200 kHz.
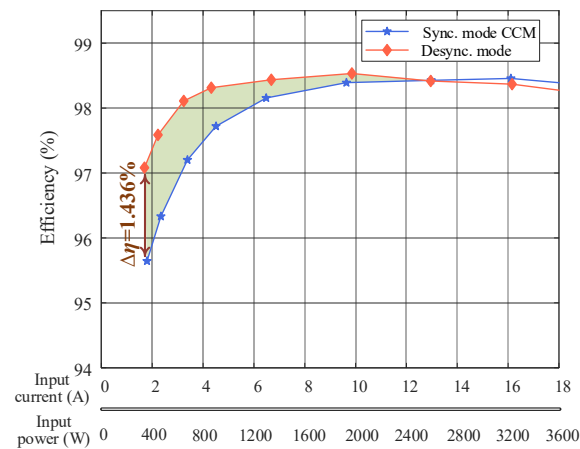

Fig. 20. Measured efficiencies of the parallel scheme when configured as a Boost dc-dc converter with different modulation schemes: synchronous CCM and desynchronized mode. The input voltage $V_{dc} = 200$ V, the duty ratio $D = 0.5$, and switching frequency f_{sw} equals 200 kHz.

The average input current is 4.25A. It can be observed that switching cell A, i.e. the leading cell, is turned on when i_{La} falls to zero while switching cell B, i.e. the lagging cell, is turned ON after the switch node voltage is discharged to 0, which indicates ZVS turn ON is achieved.

F. Validation of Power Block with Si Devices

The majority carrier device like SiC is featured by very low reverse recovery current while the loss characterization of Si devices is different. In order to validate the generality of the parallel scheme on Si devices where diode reverse-recovery loss is significant, efficiency measurement results based on Si diodes and Si superjunction MOSFET are given in Fig. 22.

In this efficiency test, the switching frequency is set as 200 kHz and it can be observed that the maximum efficiency increase: 1.23% is larger than that obtained from SiC converters (1.15%). Furthermore, the increased efficiency from desynchronized mode shows a range from 2.5A to 18A, which is larger than that from the SiC-based scheme where efficiency advantage of the desynchronized mode stops at approximately 15A. Such difference is attributed to the fact that reverse
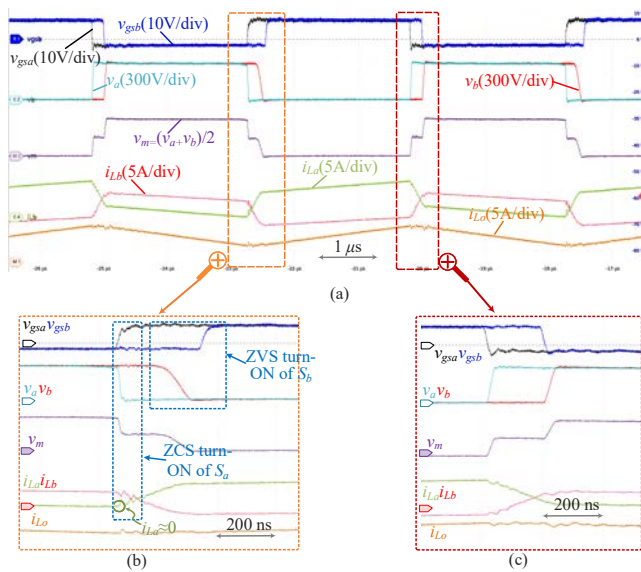
Fig. 21. Key operation waveforms of the Boost-type scheme based on parallel semi-bridge switching cells when the desynchronized mode is activated. The input voltage V_{dc} = 200 V, the duty ratio D = 0.5, and switching frequency f_{sw} equals 200 kHz. (a) Switch node voltages and inductor currents. Zoomed-in waveforms of (b) turn-ON and (c) turn-OFF transient of S_a and S_a.
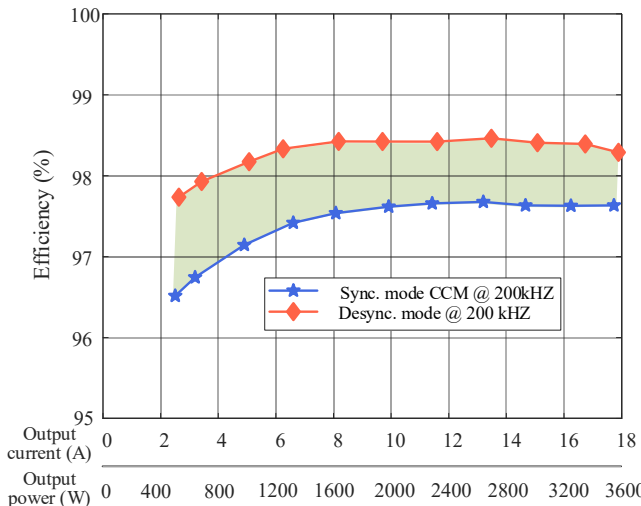

Fig. 22. Measured efficiencies of the parallel scheme when low-cost Si CoolMOS and diodes are used. The block is configured as a Buck dc-dc converter with a fixed duty ratio D = 0.5 and switching frequencies f_{sw} = 200 kHz.

recovery of the diode worsens the loss characteristic of the semi-bridge.

In Fig. 23, a comparison has been made among the SiC devices and Si devices in parallel semi-bridges in different switching schemes. As observed, the Si-based parallel semi-bridges are able to obtain similar efficiency as the SiC-based parallel semi-bridges when the desynchronized mode is used, which can be attributed to the fact that all the MOSFETs are turn-ON with ZVS or ZCS and all diodes are able to achieve ZCS turn-off, so the conduction loss dominates and the chosen Si CoolMOS has similar conduction resistance to that of SiC MOSFET. On the contrary, the efficiency of the Si parallel semi-bridges is markedly smaller than that of the scheme based on SiC devices in the synchronized mode, since
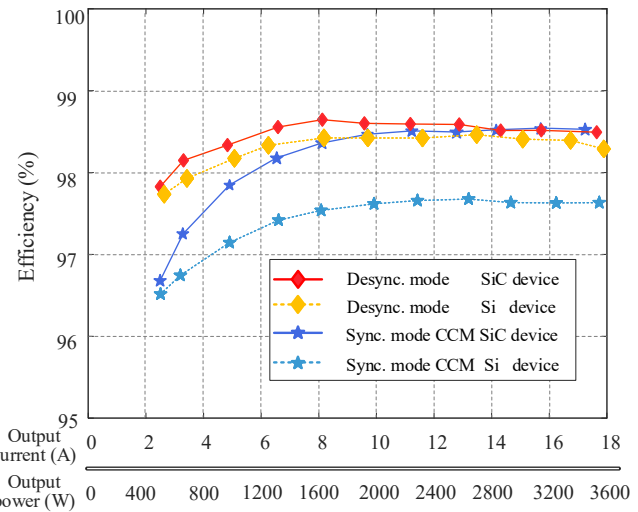

Fig. 23. A comparison between the measured efficiencies of the scheme when low-cost Si devices and SiC devices are used. The parallel switching cells are configured as Buck converters and operate at D = 0.5 and f_{sw} = 200 kHz.

SiC devices have higher switching speed and negligible reverse recovery loss. The results shown in Fig. 23 indicate that the low-cost alternative to SiC parallel semi-bridges could be of practical value and competence with the proposed scheme even compared with SiC devices in partial load by using Si CoolMOS and Si Diodes operating at desynchronized mode.

G. State Transition Between Desynchronized and Synchronized Operations

To validate the hysteresis control, experiments have been conducted with the same settings which have been used in the efficiency test in Section V-C: duty ratio D = 0.5, switching frequency f_{sw} = 200 kHz, and the input voltage is set as 400 V. In the operation transition test, the load current is switched from 14.3A to 16.1A and then back to 14.3A again. As stated in Section V-C, the efficiency of synchronized mode surpasses that of the desynchronized mode when the load current is over 15A, so 15A is set as the switching point and a current band of 0.8A is utilized to prevent undesired transition oscillation, yielding an upper band of 15.4A and a low band of 14.6A.

In Fig. 24 (a), the current and voltage waveforms of the transition process are provided. As can be seen, the circuit starts from zero output voltage. Then, the converter is in the desynchronized mode as the load current is 14.3A, lower than the upper band 15.4A. When the load current is raised to 16.1A, the load current exceeds the upper band so the synchronized mode is activated. Similarly, after the load current is reduced to 14.3A, which is less than the lower band 14.6A, the desynchronized mode is engaged. The transition from desynchronized to synchronized state can be seen in Fig. 24(b) while that from synchronized to desynchronized state is shown in Fig. 24(c). It can also be observed from the figure that the controller is able to switch seamlessly between the synchronized and desynchronized modes and the transient time are 120 μs and 135 μs, respectively, which demonstrates that fast and stable state transition could be achieved.
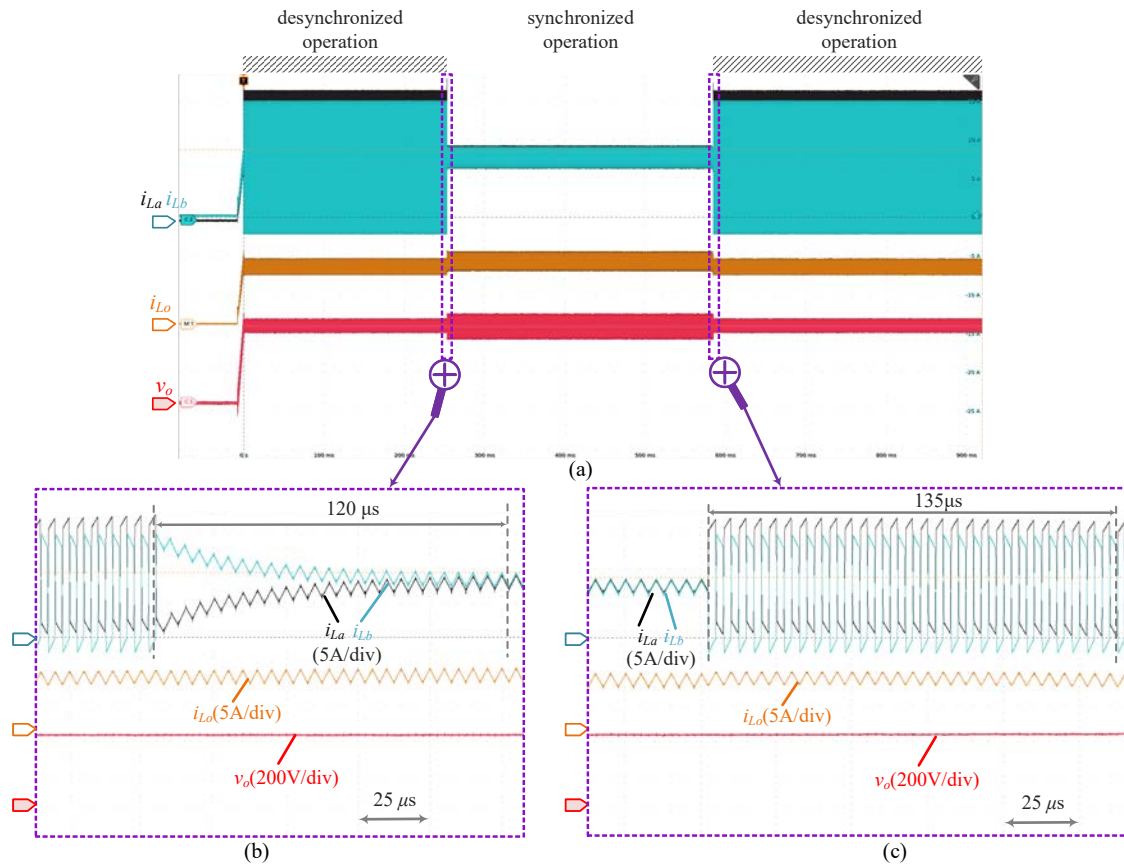
Fig. 24. Experimental waveforms during the operation mode transition process. The input voltage V_{dc} = 400 V, the duty ratio D = 0.5, and switching frequency f_{sw} = 200 kHz. The load currents at the left desynchronized mode, the synchronized mode, and the right desynchronized mode intervals are 14.3A, 16.1A, and 14.3A, respectively. The lower and higher bands of the hysteresis band are 14.6 and 15.4A respectively. (a) Output voltages and inductor currents. (b) Zoomed-in waveforms of the transition from desynchronized mode to synchronized mode and (c) zoomed-in waveforms the transition from synchronized mode to desynchronized mode.

VI. EXTENSION AND COMPARISON

A. Extension of the Proposed Paralleling Scheme

To extend the proposed method and adapt the scenario with multiple parallel switching cells, both the Buck-type and Boost-type configurations with multiple parallel switching cells are illustrated in Fig. 25.

The system is composed of N-paralleled switching cells and each one is composed of one MOSFET and one power diode. Small differential mode (DM) inductors, i.e., $L_1, L_2, \ldots, L_N$, are obtained via the leakage inductance of the PCI. Buck-type semi-bridge (Fig. 25 (a)) and Boost-type semi-bridge (Fig. 25 (b)) are adopted depending on different operation requirements. The parallel semi-bridge switching cells are divided into two groups: the leading switching cells and the lagging switching cells and the gates of leading and lagging ones are driven independently. In a multi-parallel scenario, the n_{ld} leading legs and their corresponding DM inductors are lumped into a single leading cell S_a-D_a. Similarly, the N-n_{ld} lagging cells and their corresponding DM inductors are lumped into S_b-D_b.

B. Comparison with Other Soft-switching Solutions

A comprehensive comparison among the TCM scheme for synchronous Buck converters [18], the DCM scheme for semi-bridges [16], the QCM solution [28], the ARCP method [22], and the proposed PCI-based parallel scheme is shown in Table III. Various performance metrics, including the output current ripple, switching frequency, efficiencies at light and heavy loads, and dependence on auxiliary devices and load. As can be observed from the comparison, the proposed scheme based on PCI provides a simple integration method and is able to achieve functionalities of soft switching regardless of the load condition. Moreover, the following observations can be drawn from Table III:

1) Compared to the ARCP method, no auxiliary components are required in this work so the cost and complexity of the implementation are relatively low;

2) Compared to the TCM and DCM operation, the proposed parallel scheme is able to achieve the soft-switching functionality regardless of the value of output filter and load condition, which indicates that the switching frequency is fixed and a dedicated output inductance is not required;

3) The QCM scheme is deliberately designed for HB switching cells so it is not applicable on semi-bridge switching cells;

4) Auxiliary ZVS inductor is a must for the QCM scheme. However, in this paper, the integrated magnetic design
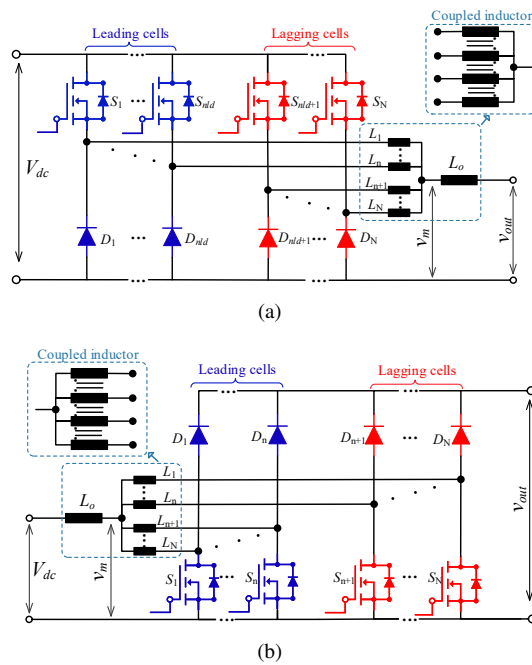
Fig. 25. Extension of the proposed scheme to multiple parallel switching cells. (a) Buck-type configuration. (b) Boost-type configuration. The leading and lagging cells can be lumped into the leading cell S_a-D_a, and the lagging S_b-D_b, respectively.

is proposed and validated where leakage inductance is used for soft switching can eliminate the ZVS inductor.

VII. CONCLUSION

A novel switching scheme of paralleling semi-bridge switching cells has been reported and verified. In this switching scheme, a small differential-mode inductance is introduced between the midpoints of paralleled semi-bridge switching cells and thus, a desynchronized modulation scheme is applied to generate a controllable circulating current that enables all devices (MOSFETs and Diodes) of the paralleled semi-bridges to achieve soft switching. The effectiveness of this paralleling scheme has been experimentally validated by a 3.6 kW Buck DC-DC converter and a 3.6 kW Boost DC-DC converter with both Si and SiC power devices. The following conclusions can therefore be drawn:

1) In this scheme, two operations modes, desynchronized mode and synchronized mode, with different loss characteristics are available and a seamless operation mode transition could be achieved for optimal full-power-range efficiency;

2) In the desynchronized mode, ZVS or ZCS turn-ON is achieved for all MOSFETs and ZCS turn-OFF is obtained for all diodes. This feature significantly reduces switching losses at partial load for both SiC and Si devices;

3) The small DM inductors are integrated into the large CM inductor required by the DC-DC converter without enlargement of the CM inductor thus no additional components are needed. The winding structure of such integrated inductor is elaborated;

4) According to the comparison among various soft-switching solutions listed in Table III, the proposed scheme provides an easy integration method and is able to achieve high efficiency by adopting desynchronized mode at partial load where switching loss dominates and synchronization mode at heavy load where conduction loss dominates;

5) In the desynchronized mode, parallel switching cells formed by Si devices (Si superjunction MOSFETs and Si diodes in this case) has higher efficiency than SiC devices in conventional synchronized switching. This feature enables a wider operation range for the desynchronized mode when low-cost Si devices are employed.

REFERENCES

[1] H. Zhao, Y. Shen, W. Ying, S. S. Ghosh, M. R. Ahmed, and T. Long, "A single- and three-phase grid compatible converter for electric vehicle on-board chargers," *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 7545–7562, 2020.

[2] Y. Jiang, M. Cheng, P. Han, Q. Wang, and X. Wang, "Analysis and dynamic control of a dual-stator bdfig-dc system supplying dc grid with minimized torque ripple through harmonic current injection," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5388–5399, 2019.

[3] Z. Chen, P. Davari, and H. Wang, "Single-phase bridgeless pfc topology derivation and performance benchmarking," *IEEE Transactions on Power Electronics*, vol. 35, no. 9, pp. 9238–9250, 2020.

[4] Z. Zeng, X. Zhang, and Z. Zhang, "Imbalance current analysis and its suppression methodology for parallel sic mosfets with aid of a differential mode choke." *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1508–1519, 2020.

[5] J. Lu, L. Zhu, G. Liu, and H. Bai, "Device and system-level transient analysis in a modular designed sub-mw ev fast charging station using hybrid gan hemts+ si mosfets," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 1, pp. 143–156, 2018.

[6] Y. Mao, Z. Miao, C.-M. Wang, and K. D. Ngo, "Balancing of peak currents between paralleled sic mosfets by drive-source resistors and coupled power-source inductors," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 8334–8343, 2017.

[7] K. Matsubara and K. Wada, "Current balancing for parallel connection of silicon carbide mosfets using bus bar integrated magnetic material," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2019, pp. 2688–2693.

[8] Y. Xue, J. Lu, Z. Wang, L. M. Tolbert, B. J. Blalock, and F. Wang, "Active compensation of current unbalance in paralleled silicon carbide mosfets," in *2014 IEEE Applied Power Electronics Conference and Exposition-APEC 2014*. IEEE, 2014, pp. 1471–1477.

[9] X. Li, L. Zhang, S. Guo, Y. Lei, A. Q. Huang, and B. Zhang, "Understanding switching losses in sic mosfet: Toward lossless switching," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*. IEEE, 2015, pp. 257–262.

[10] Y. Shen, L. Shillaber, H. Zhao, Y. Jiang, and T. Long, "Desynchronizing paralleled gan hemts to reduce light-load switching loss," *IEEE Transactions on Power Electronics*, vol. 35, no. 9, pp. 9151–9170, 2020.

[11] H. Gui, Z. Zhang, R. Chen, J. Niu, L. M. Tolbert, F. Wang, D. Costinett, B. J. Blalock, and B. B. Choi, "Gate drive technology evaluation and development to maximize switching speed of sic discrete devices and power modules in hard switching applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 4, pp. 4160–4172, 2019.

[12] S. M. Tayebi and I. Batarseh, "Analysis and optimization of variable-frequency soft-switching peak current mode control techniques for microinverters," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1644–1653, 2017.

[13] Z. Huang, Z. Liu, F. C. Lee, and Q. Li, "Critical-mode-based soft-switching modulation for high-frequency three-phase bidirectional ac–dc converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 4, pp. 3888–3898, 2018.

[14] Y.-T. Chen, Z.-M. Li, and R.-H. Liang, "A novel soft-switching interleaved coupled-inductor boost converter with only single auxiliary circuit," *IEEE transactions on power electronics*, vol. 33, no. 3, pp. 2267–2281, 2017.

TABLE III
COMPARISON AMONG VARIOUS SOFT-SWITCHING SOLUTIONS

	Synchronous Buck (TCM) [18]	Semi-bridge DCM [16]	QCM Scheme [28]	ARCP [22]	Proposed PCI-based parallel semi-bridges
Output current ripple	Large	Low - Medium	Small	Small	Small
Switching frequency	Variable, depending on output voltage and load	Constant	Constant	Constant	Constant
Partial-load switching loss	Low	Low	Low	Low	Low
Heavy-load conduction loss	High	Medium	Low	Low	Low
Soft-switching capability	ZVS for all MOSFETs	ZCS for all MOSFETs	ZVS for all MOSFETs	Main switches: ZVS Auxiliary switches: ZCS	Leading MOSFET: ZCS Lagging MOSFET: ZVS ZCS-OFF for all the diodes
Dependence on the load	Limited load range, dedicated output inductance	Limited load range, dedicated output inductance	Fixed switching frequency, independent to output inductance	Fixed switching frequency, independent to output inductance	Fixed switching frequency, independent to output inductance
Applicability	Not applicable to semi-bridge	HB semi-bridge	HB	HB&semi-bridge	Semi-bridge
Auxiliary switches	No	No	No	Yes	No
Auxiliary inductors	No	No	Yes	Yes	No

[15] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, "Ultraflat interleaved triangular current mode (tcm) single-phase pfc rectifier," *IEEE transactions on power electronics*, vol. 29, no. 2, pp. 873–882, 2013.

[16] Z. Zhang, J. Zhang, and S. Shao, "A variable off-time control method for a single-phase dcm microinverter," *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 7229–7239, 2017.

[17] Y. Wei, Q. Luo, J. Wang, and S. Pengju, "Analysis and design of the dcm operation boost pfc converter with magnetic control," *IET Power Electronics*, vol. 12, no. 14, pp. 3697–3706, 2019.

[18] W. Lee, D. Han, D. Bobba, and B. Sarlioglu, "Design of single-turn air-core integrated planar inductor for improved thermal performance of gan hemt-based synchronous buck converter," *IEEE Transactions on Industry Applications*, vol. 56, no. 2, pp. 1543–1552, 2019.

[19] Z. Zhang, J. Zhang, S. Shao, and J. Zhang, "A high-efficiency single-phase t-type bcm microinverter," *IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 984–995, 2018.

[20] Z. Ma, D. Xu, R. Li, C. Du, and X. Zhang, "A novel dc-side zero-voltage switching (zvs) three-phase boost pwm rectifier controlled by an improved svm method," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4391–4408, 2012.

[21] R. Li and D. Xu, "A zero-voltage switching three-phase inverter," *IEEE Transactions on Power Electronics*, vol. 29, no. 3, pp. 1200–1210, 2013.

[22] A. Charalambous, X. Yuan, and N. McNeill, "High-frequency emi attenuation at source with the auxiliary commutated pole inverter," *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 5660–5676, 2017.

[23] E. Chu, M. Wu, L. Huang, X. Hou, and H. Zhang, "Research on a novel modulation strategy for auxiliary resonant commutated pole inverter with the smallest loss in auxiliary commutation circuits," *IEEE Transactions on Power Electronics*, vol. 29, no. 3, pp. 1103–1117, 2013.

[24] R. De Doncker and J. Lyons, "The auxiliary resonant commutated pole converter," in *Conference Record of the 1990 IEEE Industry Applications Society Annual Meeting*. IEEE, 1990, pp. 1228–1235.

[25] J. Voss and R. W. De Doncker, "Modified auxiliary-resonant commutated pole applied in a three-phase dual-active bridge dc/dc converter," *IEEE Transactions on Power Electronics*, vol. 35, no. 2, pp. 1256–1268, 2019.

[26] G. Yao, A. Chen, and X. He, "Soft switching circuit for interleaved boost converters," *IEEE Transactions on Power Electronics*, vol. 22, no. 1, pp. 80–86, 2007.

[27] H. Wu, T. Mu, H. Ge, and Y. Xing, "Full-range soft-switching-isolated buck-boost converters with integrated interleaved boost converter and phase-shifted control," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 987–999, 2015.

[28] Y. Shen, Y. Jiang, H. Zhao, L. Shillaber, C. Jiang, and T. Long, "Quadrilateral current mode paralleling of power mosfets for zero-voltage switching," *IEEE Transactions on Power Electronics*, vol. 36, no. 5, pp. 5997–6014, 2021.

[29] R. Hou, J. Lu, and D. Chen, "Parasitic capacitance eqoss loss mechanism, calculation, and measurement in hard-switching for gan hemts," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 919–924.

[30] R. Hou, Y. Shen, H. Zhao, H. Hu, J. Lu, and T. Long, "Power loss characterization and modeling for gan-based hard-switching half-bridges considering dynamic on-state resistance," *IEEE Transactions on Transportation Electrification*, vol. 6, no. 2, pp. 540–553, 2020.

[31] G. Zhu, B. A. McDonald, and K. Wang, "Modeling and analysis of coupled inductors in power converters," *IEEE Transactions on Power Electronics*, vol. 26, no. 5, pp. 1355–1363, 2011.

[32] X. Sun, Y. Shen, Y. Zhu, and X. Guo, "Interleaved boost-integrated llc resonant converter with fixed-frequency pwm control for renewable energy generation applications," *IEEE Transactions on Power Electronics*, vol. 30, no. 8, pp. 4312–4326, 2015.

[33] R. Schlesinger and J. Biela, "Comparison of analytical models of transformer leakage inductance: Accuracy versus computational effort," *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 146–156, 2020.

[34] K. Zhang, W. Chen, X. Cao, P. Pan, S. W. Azeem, G. Qiao, and F. Deng, "Accurate calculation and sensitivity analysis of leakage inductance of high-frequency transformer with litz wire winding," *IEEE Transactions on Power Electronics*, vol. 35, no. 4, pp. 3951–3962, 2019.

[35] X. Margueron, J.-P. Keradec, and D. Magot, "Analytical calculation of static leakage inductances of hf transformers using peec formulas," *IEEE Transactions on industry applications*, vol. 43, no. 4, pp. 884–892, 2007.

[36] X. Margueron, A. Besri, P.-O. Jeannin, J.-P. Keradec, and G. Parent, "Complete analytical calculation of static leakage parameters: A step toward hf transformer optimization," *IEEE Transactions on Industry Applications*, vol. 46, no. 3, pp. 1055–1063, 2010.

[37] R. Wojda and M. Kazimierczuk, "Winding resistance of litz-wire and multi-strand inductors," *IET Power Electronics*, vol. 5, no. 2, pp. 257–268, 2012.

Yunlei Jiang (S'14) received the B.Sc. degree from Nanjing Normal University, Nanjing, China, in 2015, and the M.Sc. degree from the School of Electrical Engineering, Southeast University, Nanjing, China, in 2018. He is currently working toward the Ph.D. degree with the University of Cambridge, Cambridge, U.K., where he is jointly funded by the Jardine Foundation and Cambridge Trust.

He was a Research Assistant with the Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC), University of Wisconsin–Madison, Madison, WI, USA, from 2018 to 2019. His research interests include high-performance electrical drive based on WBG device and power electronics. Mr. Jiang is a Jardine Scholar. He was the recipient of the outstanding master's thesis of Jiangsu Province, China.

Teng Long (M'13) received the B.Eng. degree from the Huazhong University of Science and Technology, China, the first class B.Eng. (Hons.) degree from the University of Birmingham, UK in 2009, and the Ph.D. degree from the University of Cambridge, UK in 2013.

Until 2016, he was a Power Electronics Engineer with the General Electric (GE) Power Conversion business in Rugby, UK. He is currently a Lecturer with the University of Cambridge. His research interests include power electronics, electrical machines, and machine drives. Dr Long is a Chartered Engineer (CEng) registered with the Engineering Council in the UK.

Yanfeng Shen (S'16, M'18) received the B.Eng. degree in electrical engineering and automation and the M.Sc. degree in power electronics from Yanshan University, Qinhuangdao, China, in 2012 and 2015, respectively, and the Ph.D. degree in power electronics from Aalborg University, Aalborg, Denmark, in 2018.

He is currently a Research Engineer in Power Electronic at Danfoss Silicon Power, Munich, Germany. From 2019 to 2021, he worked as a Postdoctoral Research Associate at the University of Cambridge, UK. He worked as an Intern with ABB Corporate Research Center, Beijing, China, in 2015. He was a Visiting Graduate Research Assistant with Khalifa University, UAE, in 2016. His current research interests include the thermal management and reliability of power electronics, electric vehicle (EV) traction inverters, and SiC power modules.

Luke Shillaber (S'14) received B.A. and M.Eng. degrees from the University of Cambridge, United Kingdom, in 2018.

He is currently working towards a Ph.D. degree at the Department of Engineering, University of Cambridge. His research interests include high-speed switching of wide-bandgap semiconductors and high bandwidth power measurement.

Chaoqiang Jiang (M'19) received the B.Eng. and M.Eng. degrees in electrical Engineering and Automation from Wuhan University, Wuhan, China, in 2012 and 2015, respectively, and the Ph.D. degree in electrical and electronic engineering from The University of Hong Kong, Hong Kong, in 2019. He is currently an Assistant Professor with the Department of Electrical Engineering, City University of Hong Kong, Hong Kong SAR, China. He was a Postdoctoral Research Associate at University of Cambridge, U.K. Also, he is affiliated with Clare Hall Cambridge from 2021. In 2019, he was a Visiting Researcher at the Nanyang Technological University, Singapore. His research interests include power electronics, wireless power transfer techniques, electric machines and drives, and electric vehicle (EV) technologies.

Dr. Jiang is currently an Associate Editor of IET Renewable Power Generation. He has been rewarded with the Winner, CAPE Acorn Blue Sky Research Award at University of Cambridge, and First Prize in the Interdisciplinary Research Competition at University of Hong Kong.