Hybrid-Mode Adaptive Zero-Voltage Switching for Single-Phase DC-AC Conversion with Paralleled SiC MOSFETs

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***Abstract*—State-of-the-art soft-switching modulations such as critical conduction mode (CrM) and Triangular Current Mode (TCM) increase the conduction loss of power semiconductors and require variable switching frequencies, thus these soft-switching methods are seldom used in high-power DC-AC conversion. To achieve soft-switching while maintaining low RMS currents, this article proposes a Hybrid Quadrilateral and Continuous Current Mode (HQCCM) modulation for general high-frequency single-phase DC-AC conversion based on paralleled SiC MOSFETs. The proposed HQCCM adaptively operates in soft-switching Quadrilateral Current Mode (QCM) or hard-switching Continuous Conduction Mode (CCM) in one AC line cycle depending on the instantaneous AC load current. Thus, high efficiencies can be achieved over the full power range. This HQCCM modulation features adaptive soft-switching, constant switching frequency, compatibility to line filter and is applicable for high-power applications. A 4.4-kW single-phase DC-AC inverter is developed and tested to verify the advantages of the HQCCM. This article is accompanied by a video demonstrating the effectiveness of the proposed HQCCM in varying load scenarios.**

***Index Terms*—Single-phase inverter, parallel MOSFETs, soft-switching, QCM, CCM**

I. Introduction

SILLICON Carbide metal-oxide-semiconductor field-effect transistors (SiC MOSFETs) have been increasingly successful in high-switching-frequency and high-power-density applications. Although the switching loss of SiC MOSFET is reduced compared to Si counterparts, it can be still significant when it comes to high switching frequencies, and the soft-switching strategy is therefore considered as necessary to push switching frequency up to several hundreds of kHz to further increase the power density of the converter.

Extensive research has been conducted on soft-switching modulation strategies of DC-AC power converters including critical conduction mode (CrM) [1], triangular current mode (TCM) [2] [3], and discontinuous current mode (DCM) [4]. Therein, CrM and TCM are more widely discussed where the inductor current is forced to research zero or a negative value (depending on the input/output voltage ratio [2]), referred to as valley current, and resonates with the output capacitance of the switching devices. The drain-source voltage then goes down to zero before the turn-ON event, and a lossless turn-ON can be achieved. The TCM and CrM, however, increase the root mean square (RMS) current and result in higher conduction loss. The required large high-frequency current ripple [5], [6] also leads to increased inductor and conduction losses which offsets the gain of soft-switching when using CrM and TCM [7]. A significant efficiency decrease at high load has been reported thus TCM/CrM converters are mostly suitable for low-power and high-frequency applications like power factor correction (PFC) and micro-inverter [8]. Specifically, most of the studied TCM/CrM converters are approximately around 1kW [9] and the highest power reported on TCM/CrM inverters is limited to 2.5 kW [1] for single-phase systems.

Another drawback of TCM/CrM is the large switching frequency variation. As modeled and illustrated in [2], the switching frequency operating in TCM/CrM is a function of instantaneous load current and output voltage with a given power filter. This issue is particularly highlighted in the AC-tied converters as the output current is naturally sinusoidal thus the switching frequency is supposed to be continuously varying, e.g., 210kHz-500kHz in [2]. Such large variation yields excessive turn-OFF loss [3], as well as core and winding loss of the inductor [10] in high-frequency ranges. In a two-level topology, this drawback could be alleviated by swapping between bipolar and unipolar modulations [11], between CrM and DCM operations [12], between TCM and DCM [13], or implementing a variable valley current [10] or peak current [8] control to reduce the wide high-frequency range. In [14], an alternative multi-level phase bridge is used to address the issue from the perspective of topology. However, neither of those approaches keeps a real 'constant' switching frequency, but only clusters the varying switching frequencies into a smaller range [10], [11]. Meanwhile, the conduction loss deteriorates as a penalty of the smaller switching frequency range.

Furthermore, varying switching frequencies bring forward problems including electromagnetic interference (EMI) and distorted output current [15] resulting from the zero-current-detection (ZCD) circuit and also complicates the design of filter inductor and current detection. To address these issues of varying switching frequency while effectively suppress-

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ing the associated conduction loss, alternative soft-switching techniques have been proposed. In [16] and [17], a family of partial soft-switching solutions featured by quadrilateral current mode (QCM) have been proposed. These solutions are developed based on parallel-connected power transistors and manage to achieve constant switching frequency, ZCD-circuit free, and high full-load-range efficiency. Meanwhile, no auxiliary switches are required. Their advantages of wide-range efficiency improvement over conventional soft-switching solutions, e.g., CrM and TCM, have been validated with Buck and Boost DC-DC converters. However, its implementation on a DC-AC converter has not been systematically explored [18] and the adaptive mode transition between QCM and CCM, which is expected to bring forward more efficiency benefits, has not been discussed.

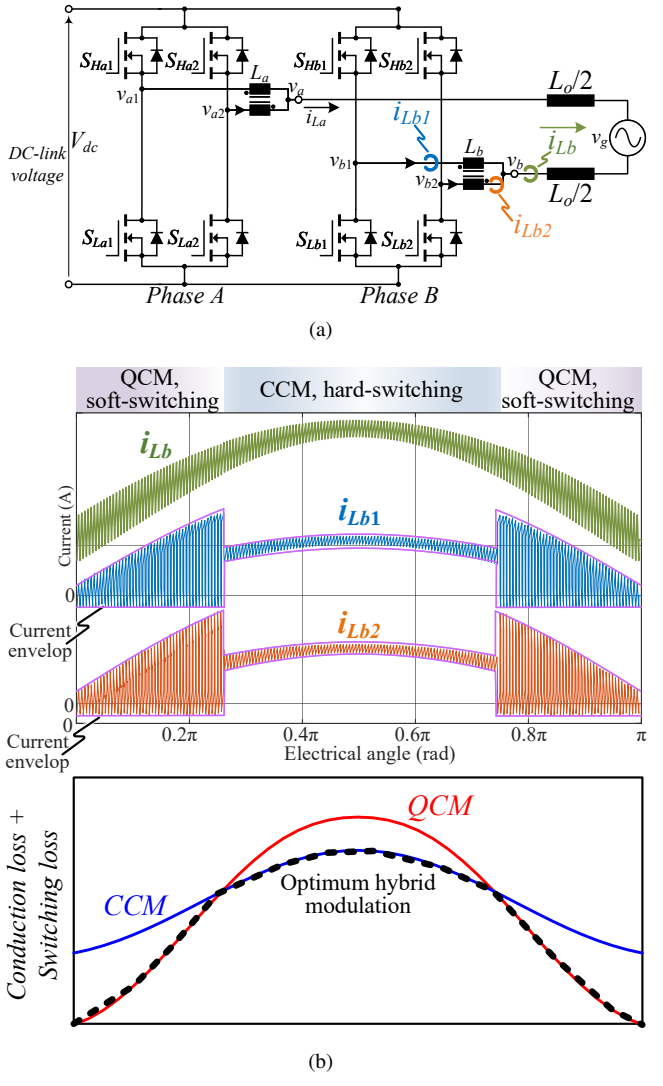

Fig. 1. Proposed topology and basic working principles: (a) Topology of the HQCCM inverter based on split parallel switching cells coupled by DM inductors. (b) Time-exaggerated view of current waveforms within half of the line cycle. CCM is activated under high load currents whereas QCM is selected below the critical current.

In light of these mentioned drawbacks in existing soft-switching solutions, this paper proposed a Hybrid Quadrilateral and Continuous Current Mode (HQCCM) modulation for H-bridge circuit in high power DC-AC conversion. Different to the TCM modulation mostly for megahertz level converters limited to low power rating applications, the proposed design intends to provide a soft-switching solution for relative high-power AC-tied applications, e.g. PV inverter, PFC and EV chargers, operating at hundreds of kilohertz [19]. This novel modulation aims to improve the efficiency at the full range of load and be compatible with the conventional CCM inverter without changes in inverter's grid connection control and grid side filter design. The contribution of this work is listed as follows:

1) Bipolar QCM, where the operation of two phases are interlocked, and its digital control implementation for DC-AC conversion are developed based on previous work on QCM [17];
2) The QCM and CCM can be seamlessly switched within one AC line cycle by the proposed HQCCM. The transition is designed at the modulation level without using additional sensors or any change of the line/output filter;
3) Theoretical analysis and proportion optimization of the proposed HQCCM scheme is developed based on the analysis of loss distribution within one line cycle. Adaptive operation depending on the instantaneous AC load current is designed for maximum efficiency at the full range of load;
4) The advantages of the proposed scheme in terms of consistently high efficiency at full range load, constant switching frequency, compatibility to conventional AC line filter, absence of complex sensors, low turn-OFF voltage stress, and reactive power capability are demonstrated and validated through experimental results by a 4.4 kW single-phase inverter. The TCM soft-switching will find difficulties in such levels of power rating due to large conduction losses and current ripples caused by its inadaptability. A comparison between the TCM and HQCCM has been provided (shown in Section III. E);

In Section II, operation principles of the HQCCM scheme, and the derivation of bipolar QCM are presented. The detailed operation optimization based on the loss distribution and mode transition is discussed in Section III, accompanied by a comparison to other solutions in terms of circuit, control and efficiency. In Section IV, a 4.4 kW prototype of which the power rating is significantly higher than other soft-switching inverters (2.4 kW in [12] and 2.2 kW in [3]), has been used to test the HQCCM. Experimental results show high efficiency, 98.3% and 98.4% at the full and half load, respectively. The conventional CCM and emerging TCM modulations for DC-AC conversion are used as the baseline to reflect the advantages of the HQCCM in this paper. Finally, the conclusion is drawn in Section V.

II. Hybrid Quadrilateral and Continuous Current Mode Modulation (HQCCM): Operation Principles

A. Proposed Topology and Key Definitions

The investigated converter circuit, shown in Fig. 1(a), allows a single-phase inverter derived from a standard H-bridge

inverter with paralleled half-bridges (or legs) to operate in the soft-switching (QCM) or hard-switching (CCM) mode, depending on the output instantaneous current. The midpoints of individual half-bridge in a paralleled group (v_{a1} & v_{a2}, v_{b1} & v_{b2}) are interconnected respectively by a reversely-coupled differential mode (DM) inductor (L_a and L_b) as shown in Fig. 1(a). The output of the DM inductor is termed as the output of the switching units, i.e. v_a and v_b, which are then connected to the grid Line and grid Neutral terminals via the output inductance (L_o), respectively. The output voltage, i.e. v_{ab}, is governed by the voltage difference between v_a and v_b.

In the proposed topology, the current difference between two parallel legs is termed as the DM current, i.e. $i_{DMa} = (i_{La1} - i_{La2})/2$ and $i_{DMb} = (i_{Lb1} - i_{Lb2})/2$. The current flowing through the filter inductors per leg, i.e. i_{La} and i_{Lb}, is termed as the common-mode (CM) current. i_{La} and i_{Lb} are of the same magnitude but opposite directions. The CM currents are governed by the output voltage v_{ab}, whereas i_{La1}, i_{La2}, i_{Lb1} and i_{Lb2} are determined by both v_{ab} and the DM voltage applied across two midpoints of paralleled legs as v_{a12} and v_{b12}.

It should be noted that the DM inductors, i.e. L_a & L_b, are typical of much lower inductance than the output filter inductance, accompanied by a relatively low volume (e.g., 17.3% of the output inductor in this work). Besides, the number of legs in parallel for each phase is theoretically unlimited, which can be accomplished by an interphase transformer network reported in [20] [21] or by lumping N parallel legs into two groups. For simplicity, two parallel legs with coupled inductors are employed for a half-bridge unit (or Phase) in this work.

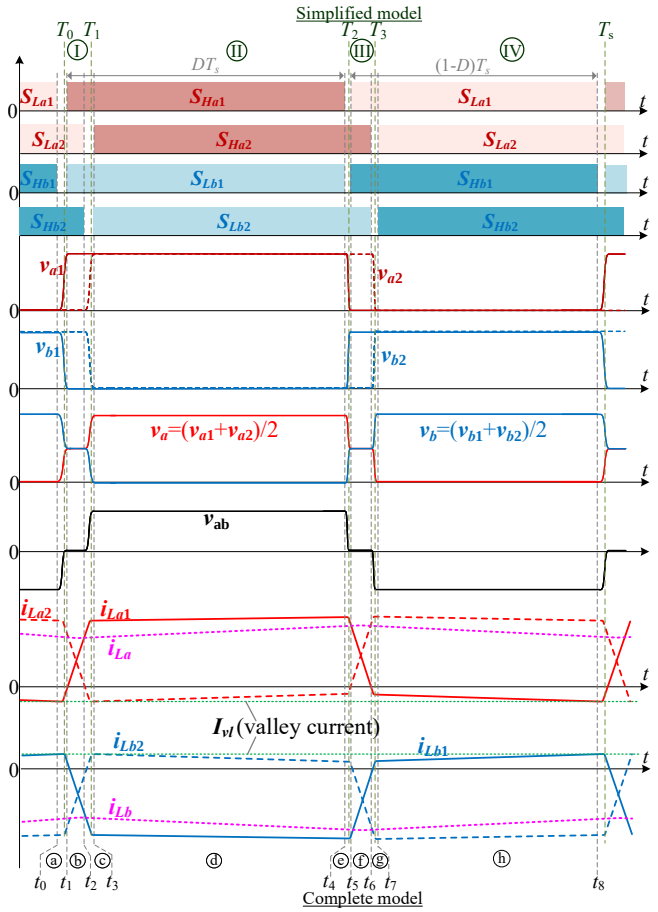

Fig. 2. Switching pattern of the proposed single-phase inverter operating in bipolar QCM (soft-switching) over one switching cycle when the load current is forward.

B. Instantaneous-Load-Current Dependent Operation of the Proposed HQCCM Scheme

For SiC MOSFET, both turn-ON and turn-OFF energy losses are composed of two portions, i.e. the current-independent capacitive loss and the current-dependent VI loss. For most commercial devices, a linear correlation between drain-source current (I_{ds}) and the current-dependent VI loss can be observed. On the contrary, an approximate quadratic correlation can be seen between the drain-source current (I_{ds}) and conduction loss, such difference leads to the observation that CCM operation is usually desired when the load current is high and conduction loss dominates, and soft-switching is preferred at the light load and high switching frequencies where switching losses are more significant.

Existing current modulation methods for grid-tied converters, including TCM and CrM, required consistent switching modes throughout different loading, resulting in low efficiency at high loads where the conduction loss is dominant. The proposed operation scheme, as seen in Fig. 1(b), allows the inverter to alternatively switch between soft-switching mode with minimized switching loss and hard-switching mode with lower conduction loss by enabling a soft-switching QCM and low RMS CCM at low and high load currents, respectively. This switching mode shift can be seamlessly achieved at not only different loads (i.e. different load current RMS values) but also within half line cycle depending on the instantaneous current value. In other words, the light and heavy loads can be segmented at a much smaller time scale (i.e. within half cycle) to minimize the switching and conduction loss for any given instantaneous AC current. Fig. 1(b) illustrates the inductor current in half line cycle: the total loss incorporating conduction and switching loss is calculated offline and a threshold is determined which marks the point when power loss of CCM is smaller than that of QCM. Although it is possible to achieve ZVS over the whole load range, the QCM is deliberately activated at a low instantaneous current and CCM is applied to the rest.

The HQCCM contains three distinct switching modes: bipolar QCM (soft-switching) mode, CCM (hard-switching) mode, and the transition mode used between the bipolar QCM and CCM mode. These three modes are adaptively applied in each half cycle of the fundamental AC period and the portion of the bipolar QCM and CCM is determined to achieve the minimum combined switching and conduction losses.

In the CCM, all the parallel devices are synchronized and the high-side and low-side devices are hard switched in the forward and reverse (c.f. Fig. 1(a)) load current directions, respectively. Since the operation of CCM has been well known, its operation analysis is not covered in this paper.

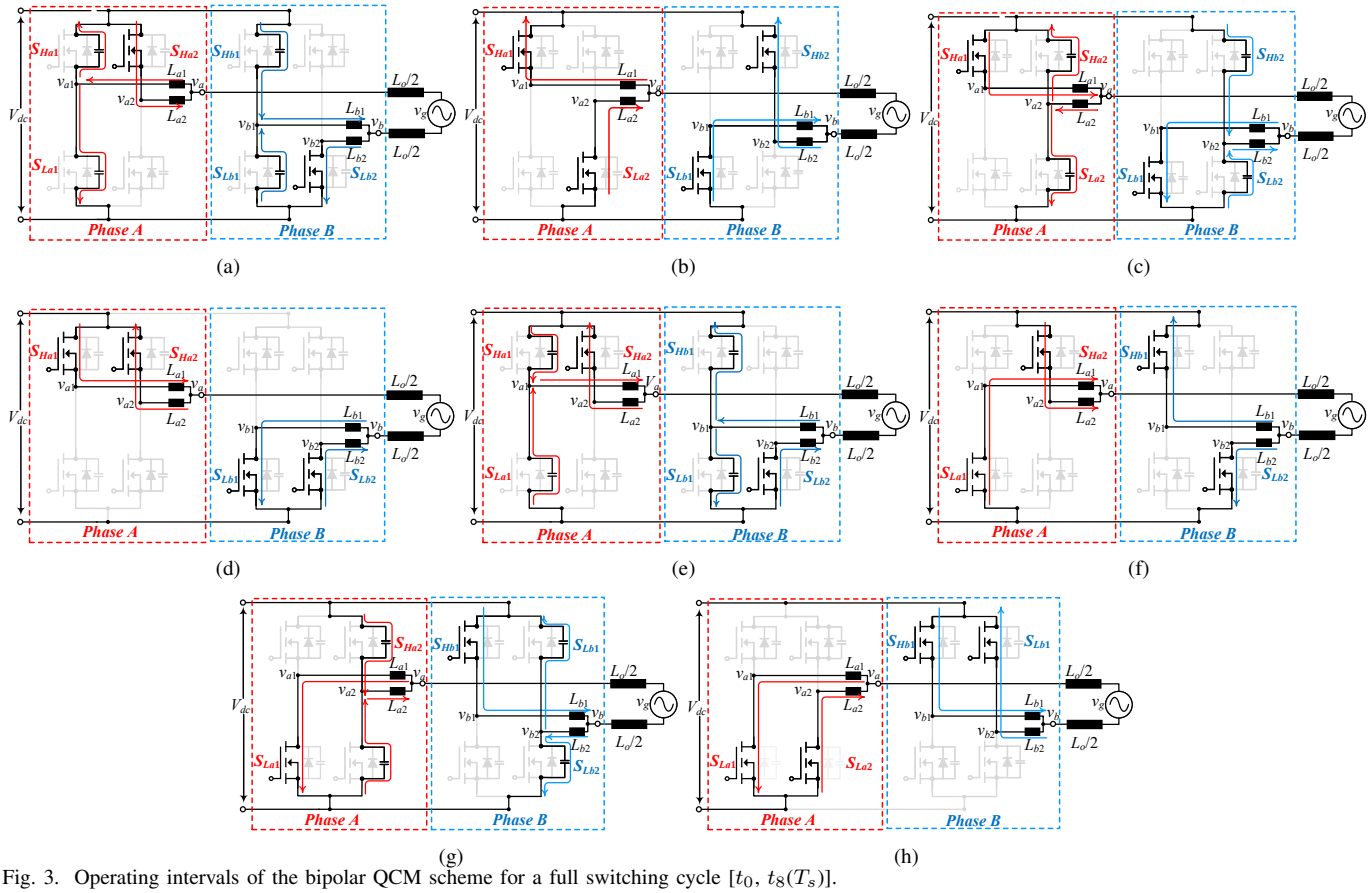

Fig. 3. Operating intervals of the bipolar QCM scheme for a full switching cycle $[t_0,\ t_8(T_s)]$.

C. Switching Pattern in Bipolar QCM

By introducing a negative inductor current on i_{La1}, i_{La2}, i_{Lb1} and i_{Lb2} before the turn-ON events of high-side devices in forward direction and low-side devices in reserve direction, ZVS-ON can be achieved for all the transistors in QCM. The operation principle of the QCM in a half-bridge with unipolar modulation has been given in [6] and this work is concentrated on the bipolar modulation where the operation of two phases are interlocked, i.e. voltage and current waveforms of these two mirror of each other.

Typical operation waveforms in the bipolar QCM operation have been shown in Fig. 2, where the gate signals for all 8 switches, inductor current through both DM and filter inductors and the switch-node voltages for a switching cycle are depicted. There are eight time intervals illustrated in Fig. 3. It should be noted that the load current (i_{La} and i_{Lb}) are assumed to be constant within one switching cycle, which is a common practice in the analysis of soft-switching behavior [11] [2].

***Interval* (a) [$t_0 \sim t_1$], ZVS turn ON of leading leg:** Before interval (a), low-side switches of phase A (S_{La1}&S_{La2}) and high-side switches of phase B (S_{Hb1}&S_{Hb2}) are conducting in opposite directions. At t_0, S_{La1} and S_{Hb1} are turned OFF and the junction capacitance of S_{Ha1} and S_{Lb1} is discharged by i_{La1} and i_{Lb1}, while switch-node voltage v_{a1} and v_{b1} begin to increase and decrease, correspondingly, to V_{dc} and 0V. At t_1, v_{a1} and v_{b1} have reached V_{dc} and 0, and the voltage across S_{Ha1} and S_{Lb1} are zero. A ZVS is therefore achieved when S_{Ha1} and S_{Lb1} are turned ON at the end of interval (a);

***Interval* (b) [$t_1 \sim t_2$], turn-ON delay ϕ_{ON} interval:** Due to different voltage at the switch-nodes of leading (subscript 1) and lagging (subscript 2) leg, DM voltage, v_{a12} and v_{b12}, pulses are applied across L_a and L_b, and the DM current is expected to increase and decrease in leading and lagging leg, respectively. The duration of the DM voltage pulse is denoted as ϕ_{ON}. By the end of interval (b), the polarity of i_{a1}, i_{a2} and i_{b1}, i_{b2} are reversed;

***Interval* (c) [$t_2 \sim t_3$], ZVS turn ON of lagging leg:** At t_2, S_{La2} and S_{Hb2} are turned OFF, and the commutation inductors L_{a2} and L_{b2} start to resonate with the output capacitors of the phase leg to which they are connected. t_3 marks the end of this resonant stage when the voltages across S_{Ha2} and S_{Lb2} reach zero, and these two switches are turned ON at ZVS;

***Interval* (d) [$t_3 \sim t_4$], positive output voltage:** During interval (d), the high-side MOSFETs of phase A and low-side MOSFETs of phase B are conducting, and the output voltage v_{ab} equals V_{dc};

***Interval* (e) [$t_4 \sim t_5$], capacitive turn OFF of leading leg:** At t_4, S_{Ha1} and S_{Lb1} are turned OFF and the commutation inductor L_{a1} and L_{b1} resonate with the output capacitors of their connected phase leg. Such process is commonly referred to as capacitive turn OFF since the channel of a MOSFET is cut off at a much higher speed than the discharging of its junction capacitor, leading to a small V-I overlapping area and low turn OFF energy. t_5 marks the end of this capacitive turn-OFF;

***Interval* (f) [$t_5 \sim t_6$], turn-OFF delay ϕ_{OFF} interval:** At t_5, capacitive turn OFF has been completed. DM voltage v_{a12} and v_{b12} with the opposite polarity to those in interval (b) are applied across L_a and L_b, again yielding the change of DM current. The duration of the DM voltage pulse is denoted as ϕ_{OFF}. By the end of interval (f), the polarities of i_{La1}, i_{La2} and i_{b1}, i_{b2} are reversed again as those in interval (b);

***Interval* (g) [$t_6 \sim t_7$], capacitive turn OFF of lagging leg:** identical to interval (d), capacitive turn OFF is achieved for S_{Ha2} and S_{Lb2} with very low turn-OFF energy in this interval;

***Interval* (h) [$t_7 \sim T_s$], negative output voltage:** During interval (f), the low-side MOSFETs of phase A and high-side MOSFETs of phase B are conducting in the opposite direction, and therefore v_{ab} equals to $-V_{dc}$.

Operation interval analysis can be summarized as: 1) the delay time between parallel legs is used to generate a DM current in the opposite direction of the load current before turn-ON events to facilitate ZVS; 2) two delay times, i.e. ϕ_{ON} and ϕ_{OFF}, are applied on the turn-ON and turn-OFF instants, respectively, and the DM currents are therefore balanced in one switching cycle; 3) With a sufficient valley current (I_{vly}) before turn-ON event (t_1&t_3), MOSFETs can achieve ZVS turn-ON, and the value of I_{vly} should meet: $I_{vly} = \sqrt{V_{dc}Q_{oss} \Big/ L_c}$ [6], where Q_{oss} is the junction charge of the SiC MOSFET implemented and L_c=L_a=L_b.

D. Simplification Model in Bipolar QCM Operation

Simplification is required to obtain the closed-form-solution of delay times, ϕ_{ON} and ϕ_{OFF}, which directly determines whether a proper valley current can be achieved to fulfill ZVS.

1) Linear MOSFET Switching Model: The nonlinearity of the output capacitance of the MOSFET has been well-known and a linear MOSFET capacitance model [2] is adopted where the switch-node voltage is modeled to behave in a discrete manner and only at two voltage levels: 0 and V_{dc}. In this model, the switch-node voltage remains unchanged until the parasitic output capacitance of the MOSFET is injected or ejected a charge of Q_{oss}. Details of the simplification process are available in [2]. With such a linear model, each nonlinear resonant stage, i.e. (a), (c), (e) and (g), can be split into two subintervals featured by linear charging/discharging behavior. Therefore, (a), (c), (e) and (g) are merged to adjacent non-resonant linear stages, i.e. (b), (d), (f) and (h) [6].

2) Closed-form Solution of Bipolar QCM Mode: Based on the linear MOSFET simplification discussed above, the QCM operation presented in Fig. 3 collapses to 4 linear switching stages, i.e. interval (b), (d), (f) and (h), which can be described by differential equations, and the mathematical description has been given as follows. For clarity, these four intervals are renamed as Stage I, II, III, and IV and are spaced apart by time instants T_1, T_2, and T_3. T_0 and T_s are the start and end of each switching period, respectively. In the mathematical description, $i_{DM} = (i_{La1} - i_{La2})/2$ and $i_{CM} = (i_{La1} + i_{La2})/2$ are used in place of i_{La1} and i_{La2} for simplicity in the following equations. For each stage analyzed below, the subscript 'T_0', 'T_1', 'T_2', 'T_3' and 'T_s' denote the time at which the values of CM and DM currents are represented.

***Stage I:* (Interval (b)) turn-ON delay ϕ_{ON}:** In Stage I, a positive DM voltage is applied across L_a and a negative DM voltage is applied across L_b. Meanwhile, the voltage difference between v_a and v_b is zero, which indicates that the CM current remains constant in this stage. Therefore, both the CM and DM currents are depicted:

$$\begin{cases} i_{CM}(t) = I_{CM,T0} \\ i_{DM}(t) = I_{DM,T0} + \dfrac{V_{dc}}{2L_c}(t - T_o) \end{cases} \tag{1}$$

***Stage II:* (Interval (d)) positive output voltage:** In *Stage II*, the high-side MOSFETs of phase A and the low-side MOSFETs of phase B are conducting and a positive DC-link voltage appears on the output. Meanwhile, the behavior of the DM current is governed by the time constant of the $R-L$ circuit along the DM path. Therefore, the analytical description of Stage II is given as follows:

$$\begin{cases} L_o \dfrac{di_{CM}(t)}{dt} = \left(\ 1 - D\ \right) V_{dc} - R_{ds,ON} \cdot i_{CM}(t) \\ L_c \dfrac{di_{DM}(t)}{dt} = -R_{ds,ON} \cdot i_{DM}(t) \end{cases} \tag{2}$$

where D is the duty ratio applied and i_{CM} and i_{DM} can be obtained by solving the differential equation (2):

$$\begin{cases} i_{CM}(t) = \frac{(1-D)V_{dc}}{R_{ds,ON}} + \left[I_{CM,T1} - \frac{(1-D)V_{dc}}{R_{ds,ON}} \right] e^{-\frac{Rds,ON}{Lo}(t-T1)} \\ i_{DM}(t) = I_{DM,T1} e^{-\frac{R_{ds,ON}}{L_c}(t-T_1)} \end{cases} \tag{3}$$

***Stage III:* (Interval (f)) turn-OFF delay ϕ_{OFF} interval:** In *Stage III*, a negative DM voltage is applied on L_a and positive DM voltage is applied across L_b. Similar to *Stage I*, the voltage across the output of the inverter is 0 as both phases are operating in delay intervals and the potential of the output terminals is therefore equal:

$$\begin{cases} i_{CM}(t) = I_{CM,T2} \\ i_{DM}(t) = I_{DM,T2} - \dfrac{V_{dc}}{2L_c}(t - T_2) \end{cases} \tag{4}$$

***Stage IV:* (Interval (h)) negative output voltage:** In the final linear stage, low-side MOSFETs of phase A and high-side MOSFETs of phase B are conducting and a negative DC-link voltage is applied on the output side. Similar to equation (2-3), the corresponding differential equation and time-domain solution can be obtained as:

$$\begin{cases} L_o \dfrac{di_{CM}(t)}{dt} = -DV_{dc} - R_{ds,ON} \cdot i_{CM}(t) \\ L_c \dfrac{di_{DM}(t)}{dt} = -R_{ds,ON} \cdot i_{DM}(t) \end{cases} \tag{5}$$

Solving equation (5) yields the time-domain expression:

$$\begin{cases} i_{CM}(t) = \frac{-DV_{dc}}{R_{ds,ON}} + \left(I_{CM,T1} - \frac{-DV_{dc}}{R_{ds,ON}} \right) e^{-\frac{Rds,ON}{Lo}(t-T3)} \\ i_{DM}(t) = I_{DM,T3} e^{-\frac{R_{ds,ON}}{L_c}(t-T_3)} \end{cases} \tag{6}$$

To obtain the closed-form solution of the circuit and solve out the analytical expressions of ϕ_{ON} and ϕ_{OFF}, two sets of initial conditions and one assumption need to be made. Since the duration of two delay widths, i.e. ϕ_{ON} and ϕ_{OFF}, bear little difference, they are therefore assumed to be the same initially, i.e., ϕ_{ON} = ϕ_{OFF}. When the steady state is achieved, the next switching cycle is initiated at T_s and we should have $I_{CM}(T_s) = I_{CM}(T_o)$, which means that the load currents at the start and end of each switching cycle are equal to each other.

Secondly, DM inductor currents, i.e. i_{La1} and i_{La2}, at T_0 and T_1 should meet the following equations to store enough energy to charge/discharge the junction capacitance for ZVS, and are used as initial conditions.

$$\begin{cases} I_{La1,T0} = I_{vl} \\ I_{La2,T0} = I_{La,T0} - I_{vl} \\ I_{La1,T1} = I_{La,T0} - I_{vl} \\ I_{La2,T1} = I_{vl} \end{cases} \tag{7}$$

where I_{vl} is termed as the minimum $I_{La1,T0}$ and $I_{La2,T1}$ allowing for complete ZVS. Substituting (7) into (1), (3), (4) and (6) yields the closed-form expression for ϕ_{ON} in (8).

$$\phi_{ON} = \left\{ -\left[2(D-1)^2 T_s - \frac{L_o T_s}{2L_c}\right] - \sqrt{\left[2(D-1)^2 T_s - \frac{L_o T_s}{2L_c}\right]^2 + (8D-4)T_s\left[\frac{2L_o I_{vl} - L_o I_{Lo}}{V_{dc}} - (D-1)DT_s\right]} \right\} / (4D-2) \tag{8}$$

where $I_{Lo} = 2\overline{i_{CM}}$ is the load current in this certain switching cycle and is obtained by calculating the averaged value of CM current in the simplified model, from Stage I to IV in one switching cycle.

Once the analytical expression of ϕ_{ON} has been obtained, we can give the expression for ϕ_{OFF} by substituting (8) into (1), (3), (4) and (6):

$$\begin{cases} \phi_{OFF} = \frac{2L_c I_{DM,T2}}{V_{dc}} + \frac{L_c}{R_{ds,ON}} W_0(A) \\ A = \frac{-2I_{DM,T0} R_{ds,ON}}{V_{dc}} \times \exp\left[R_{ds,ON}\left(\frac{(1-D)T_s}{L_c} - \frac{2I_{DM,T2}}{V_{dc}}\right)\right] \end{cases} \tag{9}$$

where W_0 is the zeroth branch of the Lambert W function and the values of $I_{DM,T0}$ and $I_{DM,T2}$ are obtained by using (1), (3) and the initial condition in (7), after knowing ϕ_{ON}.

From (8) and (9), delay times ϕ_{ON} and ϕ_{OFF} vary with the load current I_{Lo} and duty cycle D. In the control implementation, they are calculated offline and stored in two 2-D look-up tables, where load current and duty cycle serve as the input, as shown in Fig. 4, to reduce implementation effort. It can be seen from the figure that the calculated ϕ_{ON} and ϕ_{OFF} bear little difference.

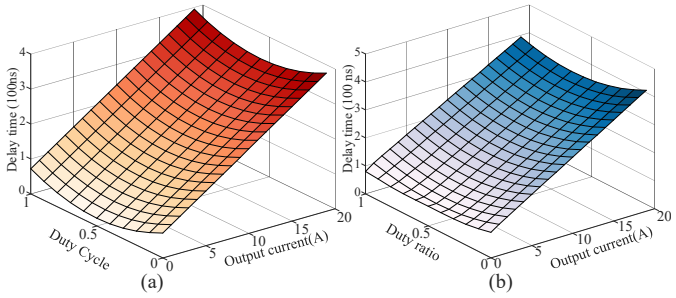

Fig. 4. 2-D look-up tables for (a) ϕ_{ON} and (b) ϕ_{OFF} versus the load current (i_{Lo}) and duty cycle (D).

E. Three-stage Output Waveform and Effective Duty Cycle

As shown in subsection II-D and depicted in Fig. 5(a), the output voltage v_{ab} of the inverter is segmented into three stages for QCM operation, namely $+V_{dc}$, 0 and $-V_{dc}$, respectively, owing to the time delays implemented. The equivalent output voltage can therefore be altered after taking the resonance and time-delay intervals into consideration. In Stage *I* (T_0 to T_1) and *III* (T_2 to T_3), where the time delays are applied, the output voltages are zero. In Stage *II* (T_1 to T_2), the output voltage is $+V_{dc}$ and the polarity is reversed in Stage *IV* (T_3 to T_s). To compensate possible distortion introduced by the resonant intervals, averaged output voltage across one switching cycle is obtained according to the voltage-second balance:

$$\overline{v_{ab}} \cdot T_s = V_{dc} T_{12} + (-V_{dc}) T_{4Ts} \tag{10}$$

where $T_{12} = D \cdot T_s - \phi_{ON}$, $T_{4Ts} = (1-D) \cdot T_s - \phi_{OFF}$, $\overline{v_{ab}}$ denotes the averaged output voltage, which can be obtained after rearranging (10): $\bar{v}_{ab} = \left(2D - 1 + \frac{\phi_{ON} - \phi_{OFF}}{T_s}\right) \cdot V_{dc}$.

In the time-delay control, the values of ϕ_{ON} and ϕ_{OFF} are close to each other and the second term of $\overline{v_{ab}}$ becomes insignificant compared to $2D-1$. Therefore, the effective output voltage mainly depends on duty cycle D. The relation between D, load current and the effective output duty cycle D_{eff} is plotted in Fig. 5, where a linear correlation that is independent of the load current can be observed. Neither the switching frequency of the converter nor the characteristics of the output voltage of the QCM are changed from the CCM thus the transfer function from voltage to current remains unchanged. This feature leads to another advantage of QCM operation in retaining the control/stability design which will be detailed in Section III. E.

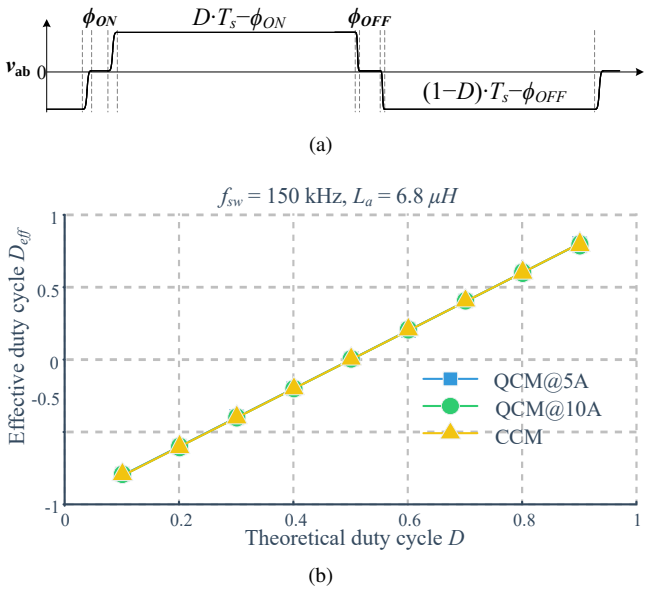

Fig. 5. Output characteristics of QCM. (a) output voltage waveform of QCM in one switching cycle. (b) voltage gain characteristic of QCM and CCM.

III. Operation Mode Transition Between QCM and CCM for Optimal Efficiency

A. Proportion Optimization between QCM and CCM

With the quadrilateral shape of inductor current i_{La1}, i_{La2}, i_{Lb1} & i_{Lb2} in QCM (see Fig. 2), the RMS current of each half-bridge over a switching period is determined by both the load and valley current. The analytical model elaborated in the last section helps to evaluate the total conduction loss induced by QCM.

The instantaneous loss distribution in QCM and CCM operation at two load conditions, half load and full load are shown in Fig. 6. At half load (2.2 kW), as shown in Fig. 6(a, b), the switching loss accounts for the highest share in CCM in half line cycle, therefore the total power loss, consisting of both semiconductor and inductor losses of CCM, is always higher than that of QCM. Such fact can be attributed to the ZVS realization of all MOSFETs which leads to negligible turn-ON loss. Meanwhile, the increase in DM inductor loss and conduction loss is relatively small and therefore QCM owns a higher efficiency over CCM across the entire half one cycle. At this load condition, QCM should always be adopted since the the loss of CCM is always higher than that of QCM.

By contrast, QCM is not always superior over CCM operation at full load, i.e. 4.4 kW. It can be observed from Fig. 6. (c) and (d) that the turn-ON loss still represents a significant portion of the total loss in CCM when the instantaneous load is small at nearby 0 and π. With the increase of the load current, the increase of semiconductor and inductor conduction loss in QCM begins to erode the benefits from the ZVS operation of QCM. The critical value, which marks the demarcation point where the total loss of QCM is higher than CCM happens at 15.6 A according to the loss calculation. Such observation hints that QCM should be adopted between 0 to 15.6 A while CCM should be chosen when the load current is higher than 15.6 A to keep the minimal total loss.

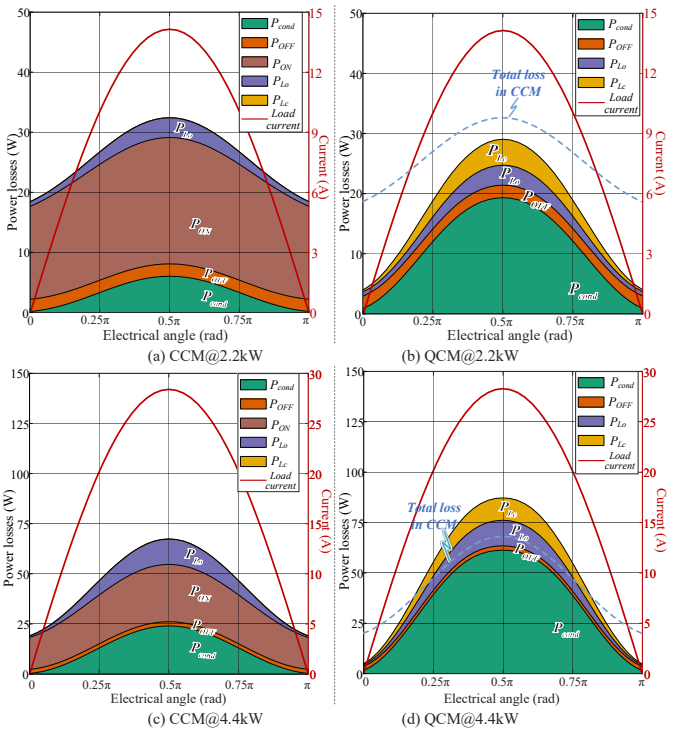

Fig. 6. Comparison of loss distribution of instantaneous power loss in half line cycle between QCM and CCM at two load conditions: (a, b) half load (2.2 kW), and (c, d) full load (4.4 kW). The core and conduction loss of the inductors are calculated using iGSE and Dowell Model [16]. The switching frequency is 150 kHz and each switch is a Cree C3M00600650K SiC MOSFET ($R_{ds,ON}$ = 60$m\Omega$). P_{Lo}, P_{Lc}, P_{ON}, P_{OFF} and P_{cond} denote the power losses of filter inductor, DM inductor, turn-ON, turn-OFF and conduction loss of SiC devices, respectively.

In Fig. 7, the portions of QCM and CCM vary while the load power is changing as illustrated. It should be noted that this figure is plotted based on unity power factor operation for the sake of clear illustration. γ is defined as $\gamma = T_{QCM}/T_{line}$ to represent the portion of QCM operation within one half line cycle, where T_{QCM} represents the duration of QCM and T_{line} is half line cycle period. As can be seen, the portion of QCM operation, γ, is 1 when the output power is smaller than 2.2 kW since QCM always enables lower power losses than CCM over the entire line cycle; γ begins to decrease when the output power exceeds 2.2 kW, reaching 0.47 at 3.3 kW, and finally standing at 0.34 at full load (4.4 kW).

B. Proposed Strategy of Mode Transition Between QCM and CCM

The benefits of operation mode transition have been clarified in the last subsection. Ideally, the HQCCM inverter has two operation modes applied to pursue the highest efficiency at any instantaneous load current at the fundamental frequency in theory by reducing both the conduction and switching losses, thus mode transition needs to be carefully handled. A hard transition from QCM to CCM causes undesirable current mismatch, as shown in Fig. 8, where the DM current remains at a high level after QCM is disabled, deteriorating current sharing between parallel devices. To solve this issue, a new switching cycle named the transition cycle (TC) is inserted

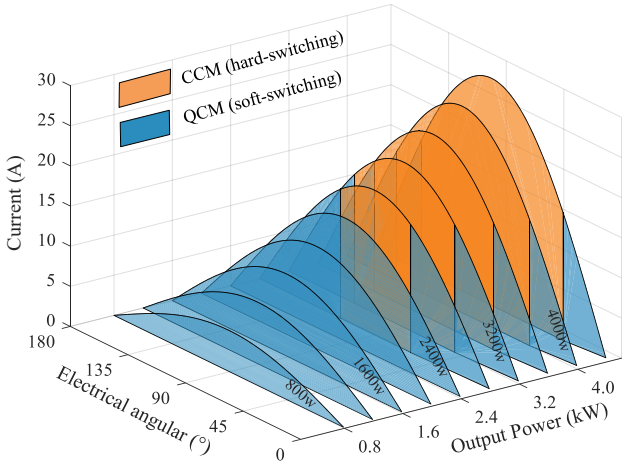

Fig. 7. Illustration of mode transition threshold and change of γ for optimized efficiency performance over half one line cycle, with varying output power.

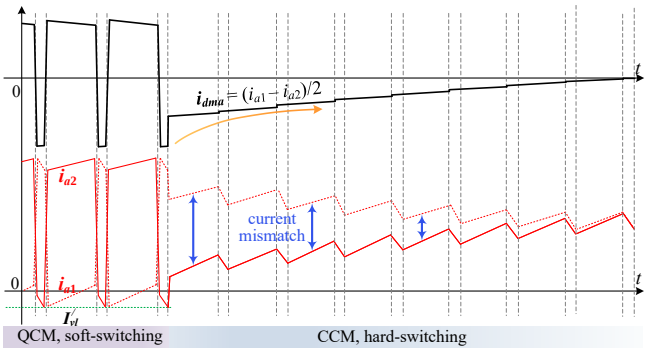

Fig. 8. Imperfect operation mode transition and the associated current mismatch without the transition cycle between CCM and QCM.

between the operation mode transition from QCM to CCM or from CCM to QCM.

Before the subsequent CCM operation starts, the DM current should decrease to zero during the TC. Therefore, the time sequence in TC needs to be designed separately from that of QCM and CCM. The current waveforms when operation mode transitions happen are illustrated are in Fig. 9 (a) and (b).

1) Mode Transition from QCM to CCM:

The TC inserted between the QCM and CCM operations is essentially an incomplete QCM state with an asymmetrical delay time.

For the TC added at the last QCM before CCM cycle, ϕ_{ON} is unchanged while ϕ_{OFF} should be shortened so that the DM current could converge from $I_{DM,T2}$ to zero by the end of the transition cycle (see Fig. 9(a)). The analytical result can be obtained by calculating the difference between I_{DMT2} and 0. In the QCM operation, the ϕ_{OFF} is defined as the duration of *Stage III* and can be analytically determined by

$$\phi_{OFF} = \frac{2\left(|I_{DM,T2}| + |I_{DM,T3}|\right) L_c}{V_{dc}} \tag{11}$$

Therefore $\phi_{OFF,TC}$ in the TC is represented by:

$$\phi_{OFF,TC} = \frac{2I_{DM,T2}L_c}{V_{dc}} = \frac{I_{DM,T2}}{|I_{DM,T2}| + |I_{DM,T3}|}\phi_{OFF} \tag{12}$$

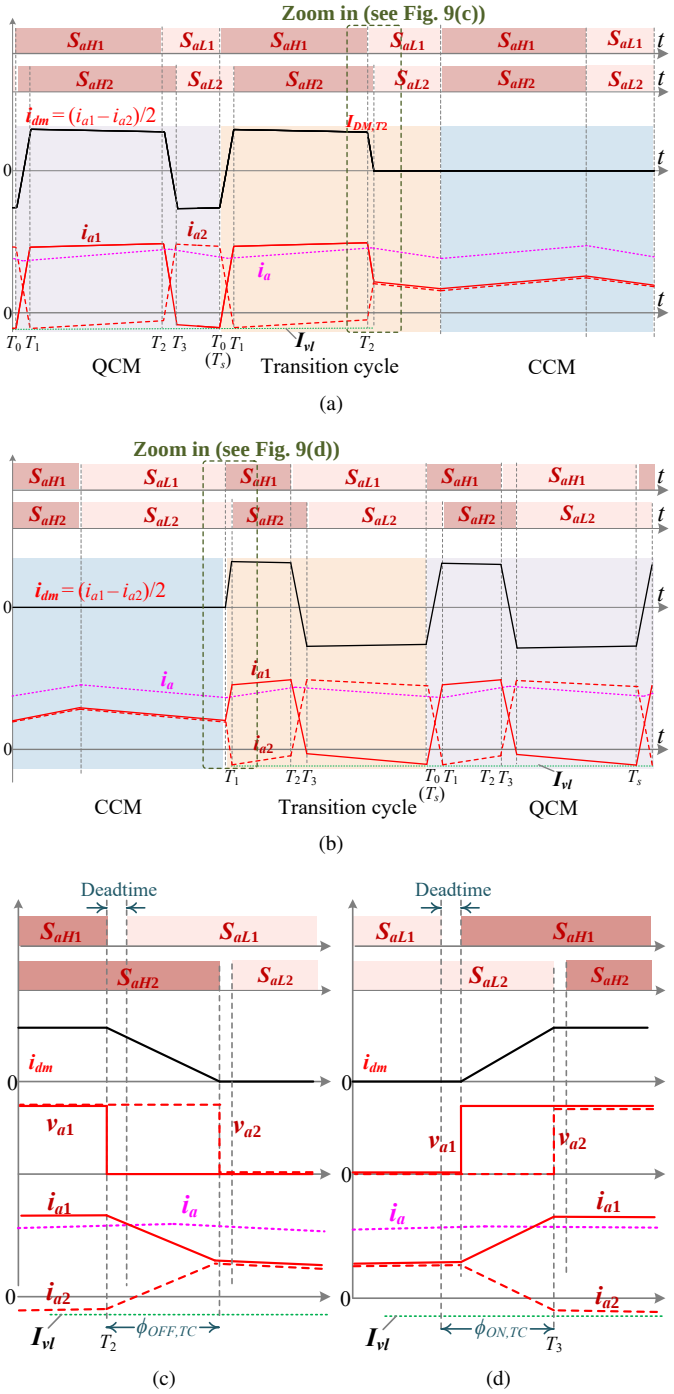

Fig. 9. Illustration of the current waveforms when operation mode transition happens from (a) QCM to CCM (zoom-in waveforms are shown in (c)) and (b) CCM to QCM (zoom-in waveforms are shown in (d)).

Note that the absolute value of I_{DMT2} and I_{DMT3} are close to each other according to (3) and (6), as the DM time constant $\tau_{DM} = L_c/R_{ds,ON}$ is large enough (∼10 times) to be outside the time scale of the switching intervals, and the DM current is therefore assumed as unchanged during *Stage II* and *IV*. Such simplification yields a straightforward but accurate result that $\phi_{OFF,TC}$ can be approximated to $0.5\phi_{OFF}$, the delay time of the last QCM cycle.

2) Mode Transition from CCM to QCM:

Similarly, when transferred from CCM to QCM, the differential current i_{DM} is expected to rise from 0 to i_{DM,T_1} by the end of *Stage I* in the TC. Therefore, $\phi_{ON,TC} = 0.5\phi_{ON}$, the delay time of the next QCM cycle, whereas ϕ_{OFF} remains unchanged.

3) Compensation of Delay Time in the Transition Cycle:

The deadtime will also lead to an imperfect mode transition. When the load current is in the forward direction (from AC switch-node) and the operation state is transferred from CCM to QCM as shown in Fig. 9(d), i_{La1} commutates from S_{aL1} to S_{aH1} with forward direction while i_{La2} commutates from S_{aL2} to S_{aH2} in the reverse direction. The difference in current direction determines whether the upper or lower device is expected to conduct during the free-wheeling period. Eventually, the actual delay time ϕ_{ON} applied is shorted due to the existence of deadtime (T_d). Therefore, ϕ_{ON} should be compensated by the deadtime: i.e., $\phi_{ON,TC} = \phi_{ON} + T_d$. A similar phenomenon happens when the load current is negative and the transition from QCM to CCM happens. ϕ_{OFF} should be compensated by a negative deadtime: $\phi_{OFF,TC} = \phi_{OFF} - T_d$.

C. Design Guidelines of Commutation Inductor and Parameter Sensitivity

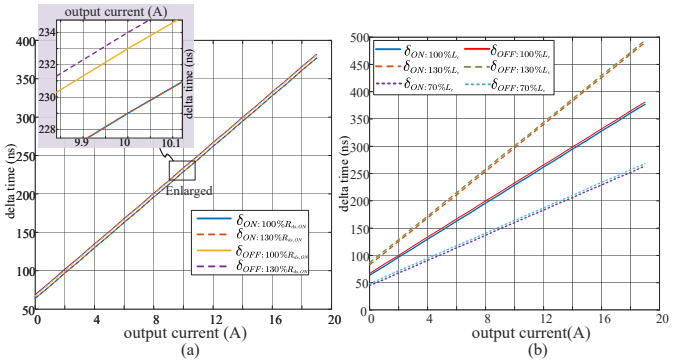

Fig. 10. Calculated time delays w/ and w/o (a) MOSFET on-state resistance $R_{ds,ON}$, and (b) commutation inductance L_c deviation.

The design of the DM inductor is expected to affect the inverter system mainly in three aspects: 1) In the CCM operation, the commutation L_c (or DM inductance or the coupled L_a and L_b) assists the parallelled devices in achieving better dynamic current sharing; 2) In QCM operation, a higher commutation inductance results in a lower valley current (see Section II. c), thus the power semiconductor conduction loss is reduced. A higher L_c value also yields a higher inductor volume and a tradeoff among conduction loss and inductor size should be made in the design of L_c; 3) Besides, the DM inductors are exposed to high fluctuations of magnetic flux density, and the core loss could be significant if the magnetic working point is selected to be too high. In this article, PQ 26/25 core is used and the turn number of the primary and secondary side of the coupled inductor is chosen to be 4, yielding a maximum magnetic field $B_{max} = 0.16T$ to limit core loss and saturation.

Meanwhile, since the control design is realized by using a 2-D look-up table shown in Fig. 4, which is an open-loop control architecture, parameter sensitivity is studied to evaluate its impact on the soft-switching realization. Both the impact of $R_{ds,ON}$ and L_c on the desired delay time are investigated in Fig. 10. As shown in Fig. 10. (a), the deviation of MOSFET on-state resistance ($R_{ds,ON}$) has a negligible effect on the delay time, suggesting that the HQCCM scheme is robust to the temperature change and the resulting $R_{ds,ON}$ variation. On the contrary, deviation of the commutation inductance (L_c) has more impacts on the delay time as shown in Fig. 10. (b). The value of L_c is monitored from the design stage by carefully keeping the working point of the core below the saturation point. Since the output current is sampled by a current sensor and the magnetic flux density within the core is zero in CCM operation, the QCM operation is opted out in the real-time control before the arrival of a load current that leads to the core saturation.

D. Control Strategy of the HQCCM for DC-AC Conversion

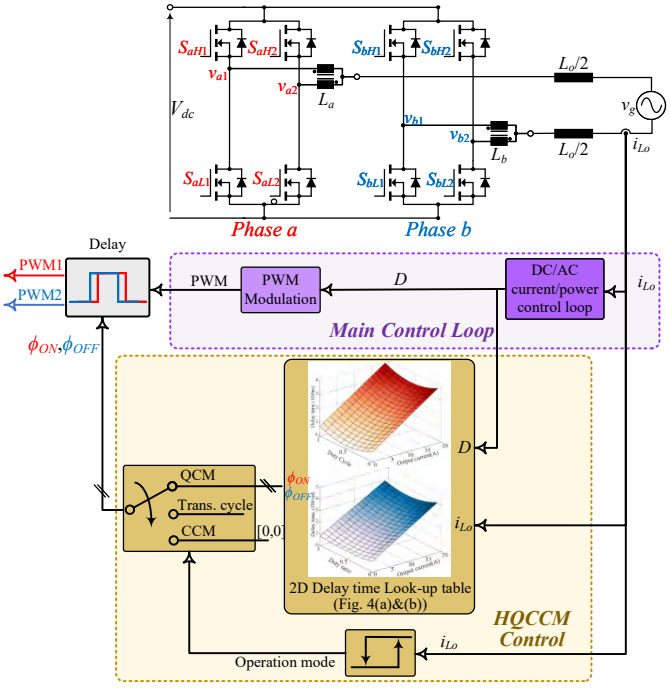

Fig. 11. Schematic diagram of the control design for a single-phase inverter using HQCCM: the hysteresis block positioned before the mode selection block helps to increase the immunity to noise.

The control design for the single-phase inverter using HQCCM has been given in Fig. 11. The HQCCM is implemented at the modulation level and the main current/power

control loop is identical to that in conventional method using CCM in a single-phase DC-AC converter, without requiring additional current or voltage sensors. Fixed control frequency (5kHz) is used and proves to provide sufficient steady-state and dynamic performance, as shown in Section IV. In the practical control implementation, undesired oscillations between two operation modes may happen due to the presence of sampling noise or overshoot during the dynamic process. Therefore, the instantaneous load current i_{Lo} at the line frequency is fed to a hysteresis block to increase the immunity to such disturbance [16]. Then, the sensed current value is feedback to the current regulator used to determine whether the CCM or QCM needs to be adapted for the minimum combined switching and conduction losses at this load current. A 2D look-up table depicted in Fig. 4 is used to generate the desired delay time between PWM pulses of parallel legs. When the immediate mode to be adapted differs from the mode used at present, a transition cycle will be inserted to accommodate the mode change between the CCM and QCM.

E. Comparison with Other Modulation Strategies in DC-AC Conversion

Characteristics of the CCM, TCM or CrM, and HQCCM for DC-AC conversion are compared and shown in Fig. 12. The HQCCM has higher efficiency and is more practical to be implemented in high power applications. Some key merits of the HQCCM strategy are elaborated below:

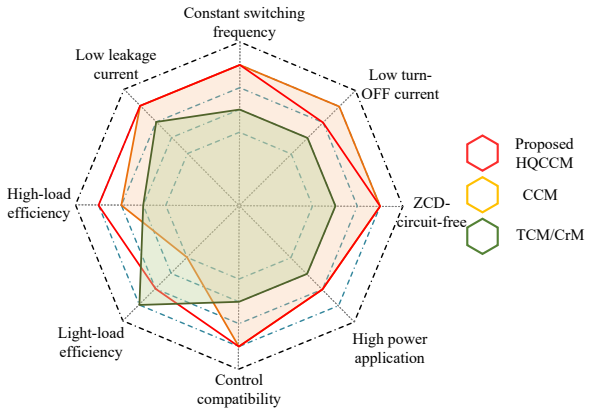

Fig. 12. Comparison of key features of the CCM, TCM and the HQCCM strategies for single-phase DC-AC conversion. The HQCCM is competitive in terms of efficiency, control and circuit.

1) Consistent high efficiency for the full range of load:

The HQCCM adapts the QCM and CCM for the minimum combined switching and conduction losses at any value of the instantaneous load current. At a high load, the QCM and CCM can co-exist in the one-half cycle of the line AC current, i.e. QCM is adapted around the zero-crossing interval and the CCM is adapted around the peak value interval. The portion of each mode in one-half cycle is also determined by the load (c.f. Fig. 7). This seamless and adaptive operation offers the HQCCM consistently high efficiency throughout the full load range.

However, the TCM or CrM cannot be opted out for high load due to the restriction of the filter hardware and control structure, thus the increased conduction loss will surpass the switching loss from the TCM or CrM. The efficiency cannot be optimized throughout the full range of load.

2) Suitable for high power applications:

The TCM or CrM trades off the conduction loss for reducing the switching loss, which is less feasible for high power applications because the conduction loss is more profound at high power, particularly for using emerging WBG devices. Instead, the HQCCM can adapt the CCM when the instantaneous current is high in order to reduce the combined conduction and switching losses. In addition, the HQCCM is designed for multiple power semiconductors connected in parallel, which is a common approach for high power rating applications.

3) Constant Switching Frequency:

Different to the TCM or CrM for DC-AC converters where the switching frequency must vary, the HQCCM achieves the constant switching frequency. This feature simplifies both the AC side filter and EMI filter hardware design and the HQCCM can use the identical filter from conventional CCM based converters.

The constant switching frequency of HQCCM also simplifies its controller design. The output current of the HQCCM is regulated by adjusting the voltage duty cycle D thus the required control bandwidth is much lower than the switching frequency. Besides, the control design of the fundamental current loop is the same as that of CCM converters. This feature preserves the benefits of traditional CCM converters in stability analysis.

However, the TCM or CrM use hysteresis-band current control and the control frequency is synchronized with the varying switching frequency via the ZCD circuit in most of the published research, although a few works have been devoted to coping with this issue [22]. This high, varying and synchronized control frequency increases the controller costs. In addition, it is more difficult to model the grid impedance and the current loop bandwidth in frequency domain due to the varying switching frequency/duty cycle. Only a little research has been put on this issue [23], [24] in a DC-DC scenario via small-signal analysis or describing function, and its behavior in a DC-AC converter where the duty cycles keep changing has not been fully revealed. Therefore, the impedance-based stability analysis [25] where the transfer function of the current regulator needs to be accurately modelled in the frequency domain cannot be easily transferred to TCM/CrM.

4) Low Turn-OFF Current and Associated Voltage Stress:

Modern WBG devices are featured by high switching speed and high di/dt which causes overshoot voltage due to the parasitic inductance in the power loop. The dependence of di/dt on the turn OFF current has been revealed in [26] and it is concluded that a higher turn-OFF current is likely to impose more voltage stress on the device. In TCM or CrM, the maximum turn-OFF current is roughly more than twice the maximum load current. In the QCM operation, the maximum turn-OFF current is only slightly higher than the load current, which significantly reduces the voltage stress applied across the device.

5) ZCD-circuit free:

The TCM or CrM operation can only be realized when

TABLE I
KEY SPECIFICATIONS OF THE 4.4-KW SINGLE-PHASE INVERTER

Part	Description Parameters	Values
SiC MOSFET C3M0060065K	Drain-source on resistance $R_{ds,ON}$	60 mΩ
	C_{oss} @ 400V	80 pF
	Maximum drain-source voltage	650 V
Main circuit	DC-link voltage V_{dc}	400 V_{dc}
	Output AC voltage v_g	220 Vrms
	Rated power P_{rated}	4.4 kW
	AC-side inductance L_a, L_b	85 μH
	DM inductance L_{a1}, L_{a2}, L_{b1}, L_{b1}	3.45 μH
	AC-side filter capacitance C_f	4.7 μF
MCU Control	Control frequency	5 kHz
	Switching frequency	150 kHz

knowing the instantaneous inductor current zero-crossing point at the switching frequency by using the ZCD circuit. Most of the TCM or CrM DC-AC converters [12], [15] rely on the ZCD circuit to detect the inductor zero-crossing point for reliable ZVS realization. In these ZCD-based control, the inductor current is regulated within the current band, but the instantaneous current sensing is reported to be error-prone [15] and lossy in high-frequency applications. For the HQCCM, however, the ZVS realization is achieved by using a 2D look-up table and the ZCD circuit is not required. The associated computational and hardware costs are eliminated as well, leading to a simple but robust control.

6) Reactive power capability:

As stated in [27], single-phase inverters are expected to support the local grid voltage with a reactive power capability, however, existing soft-switching dc-ac topologies mostly focus on unity power factor operations due to their limits of applications in non-u.p.f conditions. For example, in TCM, serious output current distortion may appear on account of a low switching frequency near the current zero-crossing point when the power factor is low. The proposed HQCCM scheme, however, naturally avoids these issues as shown in Section IV due to its constant switching frequency.

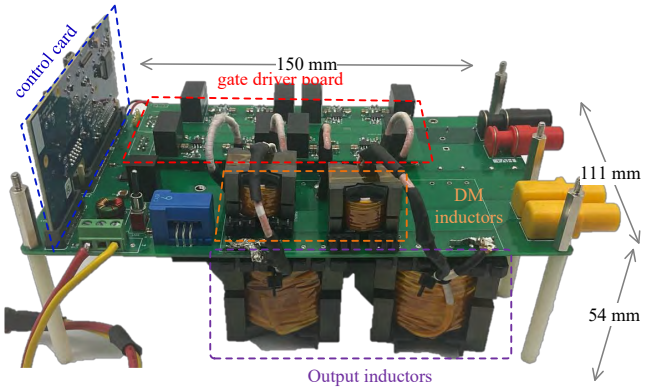

Fig. 13. 4.4 kW single-phase converter using the proposed HQCCM.

IV. EXPERIMENTAL RESULTS

A. Prototype of the DC-AC converter using HQCCM

A 4.4 kW prototype of the single-phase converter using the HQCCM scheme has been built as shown in Fig. 13. 650V SiC MOSFETs (C3M0060065) from Cree are selected as the power semiconductors for the prototype. Key details including the magnetic design and the specifications of power electronics devices are listed in Table I and the control implementation is based on a TI TMS32028379 control card. Since the maximum current rating of SiC MOSFET is determined by the maximum junction temperature, which is partially determined by the power losses, the power rating of the HQCCM inverter would be higher than a conventional CCM inverter with identical devices. Eventually, the power density of the converter is 4.89 kW/L, excluding the control card and DC link capacitors. Note that the control frequency of the converter is much lower than the switching frequency, which would not be possible in TCM or CrM converters with variable switching frequencies.

B. Steady-state Dynamic Experimental Waveforms

The measured drain-source and gate-source voltages of the inverter operating in the bipolar QCM mode are shown in Fig. 14. When the load current direction is forward for phase A, i.e. reverse for phase B, ZVS is expected to be achieved on the upper device of phase A (S_{Ha1}&S_{Ha2}) and lower device of phase B (S_{Lb1}&S_{Lb2}) (c.f. Fig. 1). Meanwhile, the remaining devices can inherently achieve ZVS. As can be seen from the zoom-in waveforms in Fig. 14 (c) and (d), where the waveforms for phase A and B are demonstrated respectively, the drain-source voltages have decreased to 0 before the rising of the corresponding gate-source voltage. Specifically, switch-node voltages v_{a1} and v_{a2} both increase to V_{dc} in Fig. 14 (c) before the gating of upper devices, i.e. v_{gSa1H} and v_{gSa2H}, indicating the drain-source voltages of S_{aH1} and S_{aH2} have been discharged to zero and ZVS-ON is realized for upper devices. Similarly, zero switch-node voltages v_{b1} and v_{b2} can be observed before the gating of v_{gSa1L} and v_{gSa2L} and ZVS-ON can be therefore confirmed as well.

Fig. 14 depicts the experimental steady-state waveforms of the HQCCM inverter under various load conditions: light (1.4 kW), partial (2.78 kW) and full (4.4 kW) load. In this figure, currents of the DM inductors, i_{La1}, i_{La2}, i_{Lb1} and i_{Lb2}, the CM inductor, i_{La}, and the grid-side voltage v_g are shown. The portion of QCM operation, i.e. the value of γ, is 1 at light load since the peak load current is below the transition threshold current. When the load increases, however, γ, decreases to 0.61 at partial load and finally to 0.36 at full load, where CCM is more beneficial for the higher load current. It can also be seen that the valley current remains to be constant and stable regardless of the sinusoidal load current, which verifies: 1) the accuracy of the analytical model, 2) the correctness of the model simplification, 3) the feasibility of the mode transition compensation strategy, and 4) the effectiveness of the look-up table (c.f. Fig. 4). Note that all the soft-switching operation is achieved without any auxiliary circuit (e.g. ZCD or v_{ds} detection) which is a must for traditional TCM/CrM soft-switching converters.

C. Reactive Power Capability

Fig.16 presents the experimental results under the non-unity power factor condition. In the test, the power factor is deliberately adjusted to 0.4 ($\phi = 66°$), indicating that the

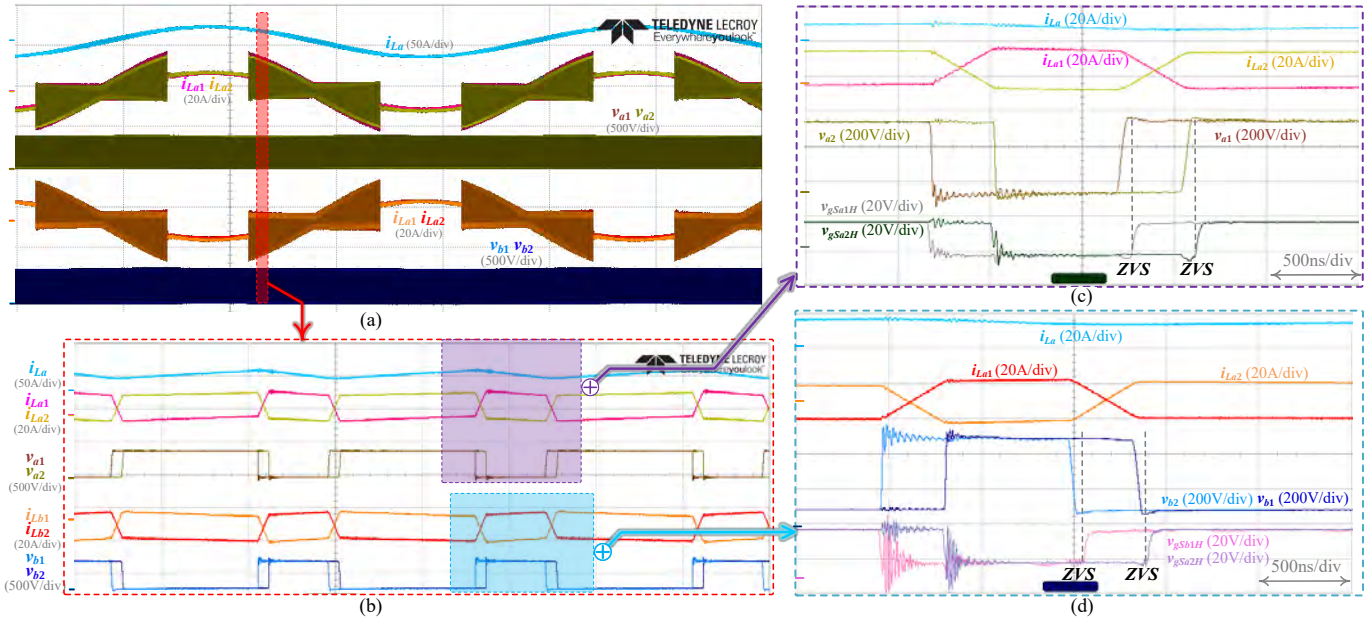

Fig. 14. Key current and voltage waveforms of the HQCCM DC-AC converter demonstrating the ZVS operation under QCM operation at partial load: P_o=2.5 kW and γ = 0.72. (a) Full picture. (b) Zoom-in waveforms @ i_{Lo} = 12A (time scale: 2 μs/div). Zoom-in waveforms of phase (c) A and (d) B (time scale: 500 ns/div).

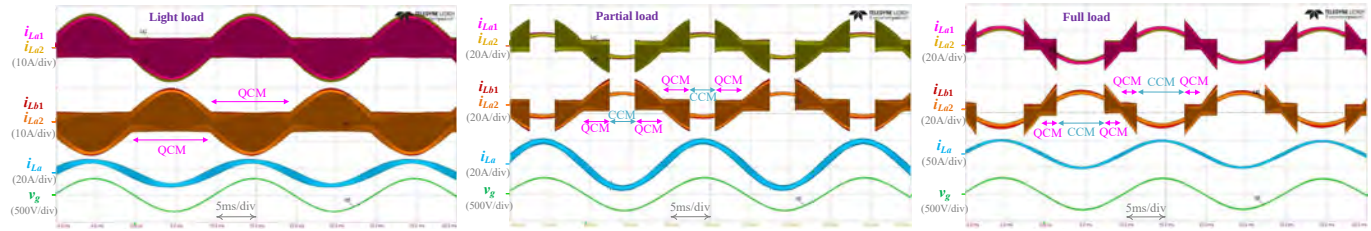

Fig. 15. Experimental steady-state waveforms at (a) light load (1.4 kW), (b) partial load (2.78 kW) and (c) full load (4.4 kW).

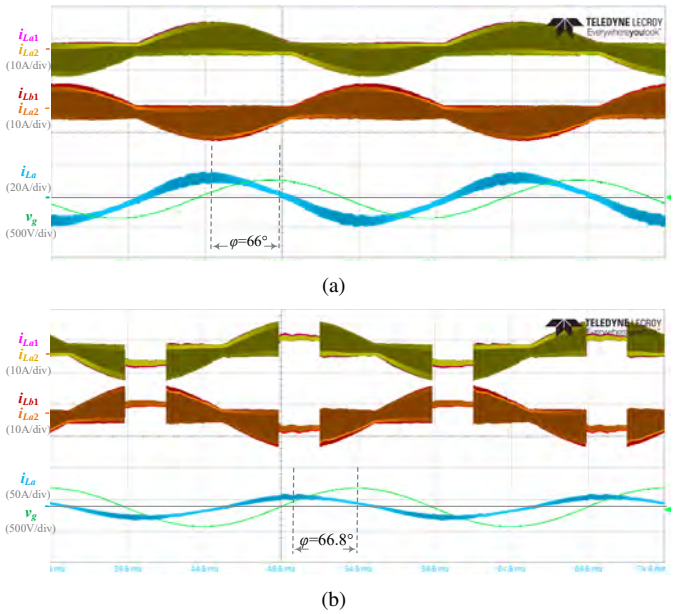

Fig. 16. Experimental results at PF=0.4. (a) apparent power = 2120 VA, active power = 850 W, and reactive power = 1942 Var; (b) apparent power = 2500 VA, active power = 1000 W, and reactive power = 2291 Var.

reactive power fed to the grid was larger than the active counterpart. Such operation condition happens when the inverter is instructed to support the local grid voltage. The reactive power capability is verified at two conditions. In Fig. 16. (a), apparent power was set to S=2120 VA and only QCM was implemented. At the same p.f., the apparent power was increased to S=2500 VA in Fig. 16. (b) when both QCM and CCM were activated within one line cycle due to a higher load current. It can be seen from Fig. 16 that the proposed HQCCM scheme is able to handle both unity and non-unity power factor conditions at different load currents.

D. Mode Transition and Step Load Dynamic Waveforms

Fig. 17 shows the dynamic voltage and current waveforms under a step load change with the proposed HQCCM scheme. In the experiment, the load power was increased from 1.5kW to 3.5kW and these step load changes have been applied at two moments to have two different occurrence of electrical angles. In Fig. 17. (a) and (b), the load step happened at approximately $\pi/3$ electrical angle and the inverter was entirely in QCM operation prior to the load increase. The operation mode was subsequently switched to CCM after the step, due to an increase of peak-peak current from 19A to 45A. In the

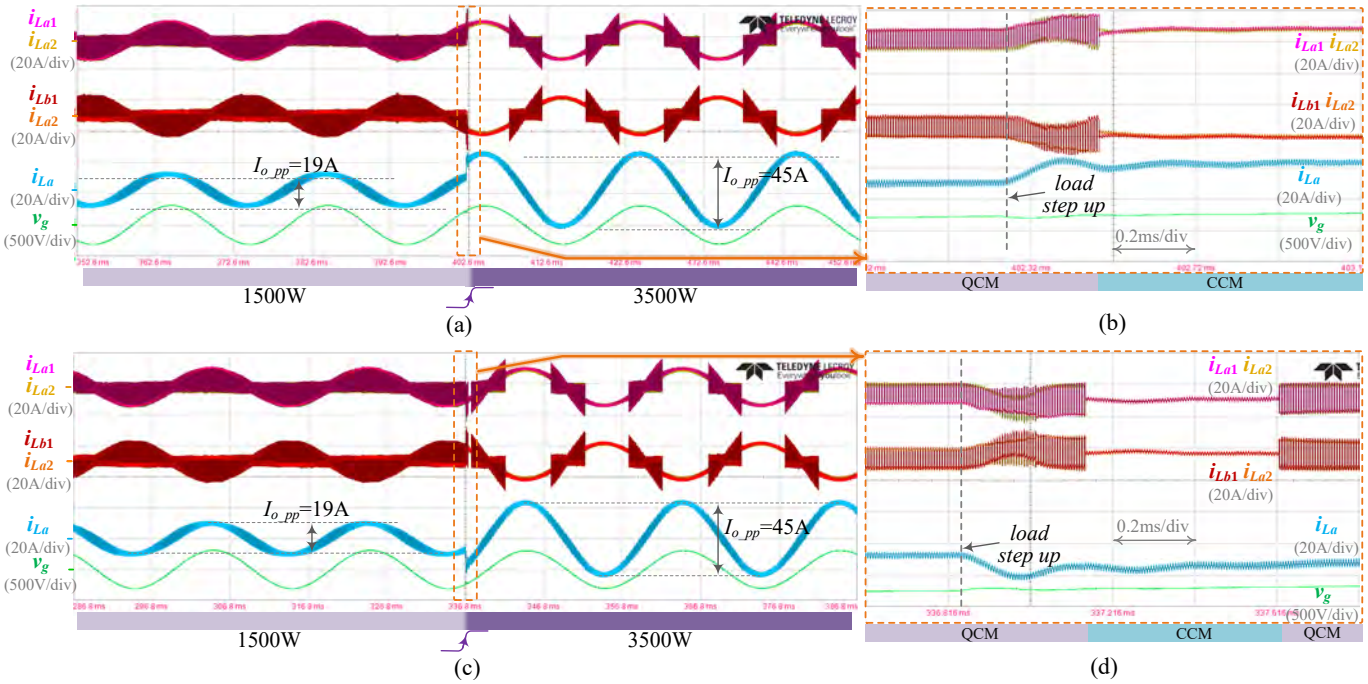

Fig. 17. Measured dynamic waveforms of the HQCCM scheme under step load changes at random electrical angles over one period. The input voltage $V_{dc} = 400V$ and the output voltage $V_{oRMS} = 220V$. The output power increases from 1500W to 3500W at (a) approximately $\pi/3$ electrical angle of the cycle and (c) approximately $5\pi/6$ electrical angle. Zoom-in waveforms of (a) and (c) are demonstrated in (b) and (d), respectively.

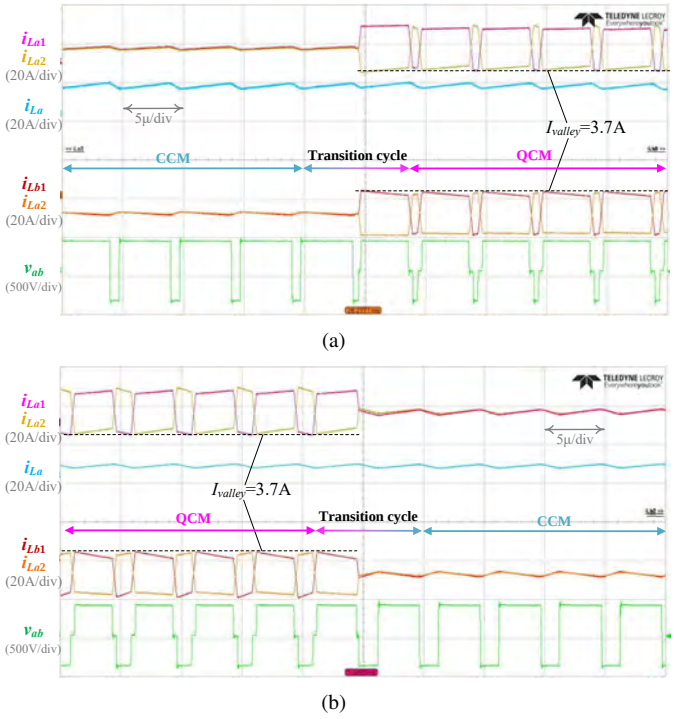

Fig. 18. Measured waveforms during operation mode transition when the switching frequency is set as 200 kHz: (a) from CCM to QCM and (b) from QCM to CCM.

following line cycles, the QCM was alternatively activated with the CCM based on the optimal efficiency operation at this 3.5kW load. In Fig. 17.(c) and (d), a similar load step was applied at approximately $5\pi/6$ electrical angle of the cycle. The operation mode shortly experienced CCM due to the load increase then entered QCM again because the occurrence of load change was close to the zero line current of that cycle. A small delay in response can be observed as fixed control frequency (5 kHz) is used, and the controller requires one cycle to sense current and update the PWM signals . It can be also seen from Fig.17(a)-(d) that the described mode transition control in Fig. 11 is able to achieve a smooth mode transition in spite of the complexity of the operation condition.

In the demonstration video accompanying the article, a 60-second continuous test is conducted and the load power is sequentially increased from 0.8kW to 1.8kW, to 2.6kW and finally to 3.4 kW. The demonstrated experimental results further validate the effectiveness of the mode transition strategy.

In Fig. 18, enlarged current and voltage waveforms are shown to depict the operation mode transition process. As discussed above, the mode transition is expected to happen when the load current moves across the transition current point (14.5 A with the power semiconductors and inductor design listed in Table I). It can be seen from the figure that the transition process is smooth with minor current mismatch after entering into the new operation state, with the aid of the transition cycle. Another observation on the output waveform is that v_{ab} appears to be a three-level waveform in QCM and a two-level waveform in CCM, as stated in Section II.

E. Measured Efficiency of the Prototype Utilizing the Proposed HQCCM Scheme and Loss Breakdown

The efficiency curve of the HQCCM inverter, which is measured by a Yokogawa WT5000 power analyzer, and its comparison to QCM, CCM and TCM schemes are plotted in Fig. 19. When compared with QCM and CCM, the HQCCM scheme owns the highest efficiency across the whole load

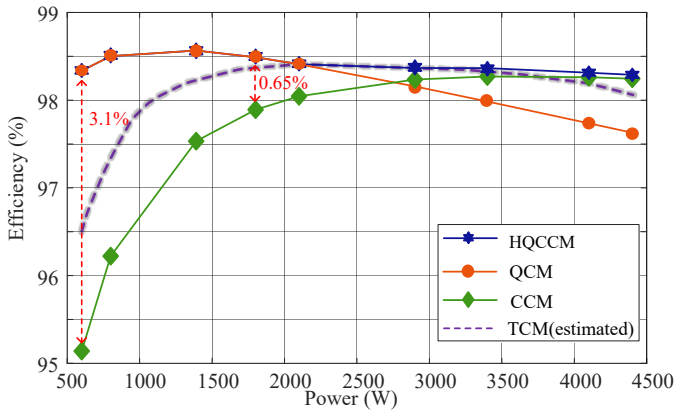

Fig. 19. Measured efficiency curve of the HQCCM inverter and a comparison to QCM and CCM scheme.

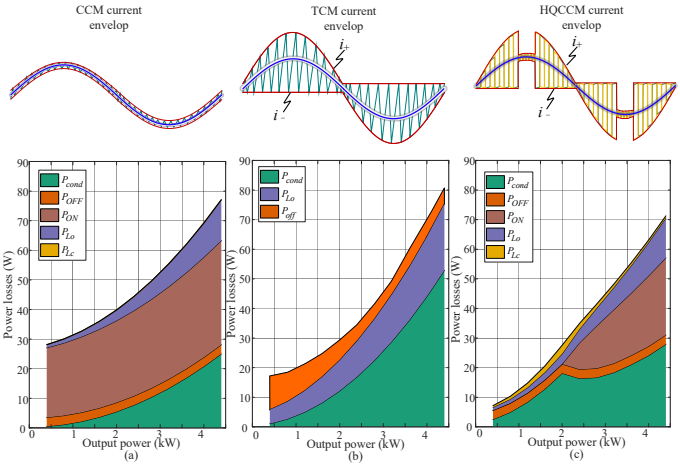

Fig. 20. Comparison of loss distribution among three schemes: (a) CCM, (b) TCM, and (c) HQCCM.

range. The peak efficiency of the inverter is 98.55% which occurs at 1440W but remains almost constant across the whole load range. The HQCCM has the identical efficiency of the QCM at partial load when $\gamma = 1$ and much higher (3.1% higher) efficiency than CCM since the major switching loss has been eliminated by ZVS. When the load is relatively high, i.e. $\gamma < 1$, the HQCCM shows a moderate efficiency increase because the switching loss is still reduced but the conduction loss is more significant.

Fig. 20, where the loss breakdown of TCM, HQCCM and CCM are given, provides a direct view of the loss distribution at various load conditions. The comparison is based on the identical semiconductor configuration listed in Table I (two 60 mΩ SiC MOSFETs in parallel). At light loads, the TCM suffers from high switching frequency and associated inductor loss and turn OFF loss. The total loss is therefore higher than that of HQCCM. When the load increases, both the conduction loss of QCM and TCM increase correspondingly. However, the HQCCM scheme is able to return back to CCM at high instantaneous load current, thanks to its adaptive and smooth operation mode transition capability. Therefore, the increase of conduction loss in HQCCM is successfully suppressed whereas that of TCM is keeping increasing. At full load, the combined conduction and inductor loss of TCM is obviously higher than that of HQCCM. Overall, the proposed HQCCM scheme is able to achieve a better efficiency performance over CCM and TCM in single-phase inverters. Note that the given loss estimation of TCM is calculated based on a conventional modulation with constant lower i_- current band of the current envelop, as shown in Fig. 20(b). Although numerous other schemes for TCM has been introduced, the constant-lower-band modulation scheme stands out as the most representative one [28] and is therefore used as the benchmark here.

V. Conclusion

This paper proposes a Hybrid Quadrilateral Continuous Current Mode (HQCCM) modulation for single-phase inverters constructed by parallel half-bridges. Based on the fact that switching loss is more dominant than conduction loss at light load and this pattern is reversed at high load, the proposed solution designs a modulation scheme where soft-switching and hard-switching can be alternatively adopted depending on the instantaneous value of output current for optimal efficiency performance. By taking both switching and conduction loss into consideration, the optimal mode transition threshold is chosen to maximize the efficiency. The proposed HQCCM solution features high efficiency over full-load, constant switching frequency and ZCD-circuit free. In addition, the HQCCM is fully compatible with the conventional line filter design and control stability criteria. A 4.4 kW prototype with 4.89 kW/L power density has been built for experimental validation, and a constantly high efficiency within the entire load range can be observed. The advantages of this adaptive ZVS could potentially set a new design principle and figure-of-merit for selecting power electronic devices for high-frequency power converters.

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