

Analysis and Design of a Novel Six-Switch Five-Level Active Boost Neutral Point Clamped Inverter

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Abstract— This paper presents an analysis and design of a new boost type six-switch five-level Active Neutral Point Clamped (ANPC) inverter based on switched/flying capacitor technique with self-voltage balancing. Compared to major conventional 5-level inverter topologies, such as, Neutral Point Clamped (NPC), Flying Capacitor (FC), Cascaded H-bridge (CHB) and Active NPC (ANPC) topologies, the new topology reduces the dc-link voltage requirement by 50%. Whilst reducing the dc-link voltage requirement, the number and the size of the active and passive components are also reduced without compromising the reactive power capability. The analysis shows that the proposed topology is suitable for wide range of power conversion applications (for example, rolling mills, fans, pumps, marine appliances, mining, tractions, and most prominently grid-connected renewable energy systems). Experimental results from a 1.2-kVA prototype justifies the concept of the proposed inverter with a conversion efficiency of around $97.5\% \pm 1\%$ for a wide load range.

Index Terms—Multilevel inverter, Active-Neutral-Point Clamped (ANPC) Inverter, Flying Capacitor, Pulse-Width-Modulation (PWM)

I. INTRODUCTION

MULTILEVEL inverters exhibit some interesting advantages compared to two-level VSIs, especially for higher voltage power conversion, where lower switch voltage stress and lower harmonic content exist. For grid-connected application, for example, photovoltaic inverters and motor drives, multilevel topologies are more common due to their advantages regarding an improved output current, lower switching losses and reduced electromagnetic interferences. In multilevel topologies low voltage switches can be used instead of high voltage switches as in two-level inverters. Low voltage switches are normally smaller and cheaper and they can handle higher switching frequencies. In addition, the conduction losses can be reduced with the application of low voltage switches with lower collector-emitter saturation voltage ($V_{CE,sat}$) and/or low drain-source ON resistance ($R_{ds,on}$). Though the number of switching devices increases in multilevel converters, the switching loss is also reduced due to lower switching frequency. To achieve the same output power quality in two-level topologies, they need to switch more often than multilevel topologies; thus the switching frequency can be reduced in multilevel topologies, which reduces

the switching losses. To improve the output voltage waveform, multi-level topologies offer more than two voltage levels. Various multilevel converter topologies have been reported in the literature since 1970s [1]. Subsequently, several multilevel converter topologies have been developed with different features. The most popular conventional multilevel topologies which have found wide industrial applications includes: diode neutral point clamped (NPC) converter [1]–[5], [9], flying capacitor (FC) converter [5]–[7], cascaded H-bridge (CHB) converter [3], [8], [11] and hybrid structure consisting of H-bridge and NPC and/or FC topologies [8], [11] and [12]. Fig. 1 shows different conventional 5L-inverter topologies. With several voltage levels, a better approximation to a sinusoidal waveform can be achieved which comes with a reduction in the passive filter components and therefore a lower THD. However, besides these advantages, the main drawbacks of multilevel inverters are their complexity regarding the structure and control technique. For example, the voltage level in NPC can be increase, but the number of clamping diodes and capacitors also increase, which increase losses and size of the converter. Furthermore, dc-link capacitor voltage balance becomes unattainable in higher-level NPC topologies demanding complex control strategy [3]. Similarly, CHB requires a large number of isolated dc sources or requires to be fed from phase-shifting isolation transformers. This makes the system more bulky and expensive [2], [3]. Likewise, a more complex control scheme is required to balance the voltage of each capacitor in the higher-level FC type topologies [5], [6] and [13].

In addition to the above complexity, generally multilevel inverter requires a higher dc-link voltage, which is two times the peak of the ac output voltage as shown in Fig. 2. For many applications, the traditional designs may require an additional boost converter in the input or a step-up transformer in the output. For example in the European grid, the dc-link voltage should be at least $2 \times 230 \times \sqrt{2} \text{ V} = 650 \text{ V}$ (theoretical value, in real application this value will be higher due to tolerances). However, the multi-stage power conversion reduces the efficiency and reliability, whilst increasing the size and cost of the system. The additional boost stage can be eliminated by connecting PV modules in series (string) to produce a higher dc-link voltage, whereas the losses due to mismatch between the modules and shading relatively forfeits the energy gain from the system. Therefore, a single-stage dc-ac power converter with boost capabilities offers an interesting alternative compared to two-stage approach [14].

ANPC topologies, which combine the concept of NPC, FC and/or CHB have received more attention in the recent time for medium power applications as they retain most of the advantages of the parent topologies [4], [6], [12], [16] and [19]. An interesting cellular based hybrid topology with flying capacitor is presented in [20] using single dc-power source where output voltage in MMC configuration is higher than the input voltage. However, the higher dc-link voltage requirement [4], [6], [12], [16] and [19] and more active and passive components still demands an enhanced circuit topology with improved overall system efficiency, reliability, power density and lower cost to

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make it more attractive and competitive than the classical topologies. Considering this aspect, a novel six-switch five-level boost-ANPC inverter (5L-Boost-ANPC) is investigated for general-purpose applications (for example, rolling mills, fans, pumps, marine appliances, mining, tractions, and most prominently grid-connected renewable energy, etc.), which reduces the dc-link voltage requirement to half of the conventional 5L-NPC and 5L-FC family, whilst reducing both active and passive components.

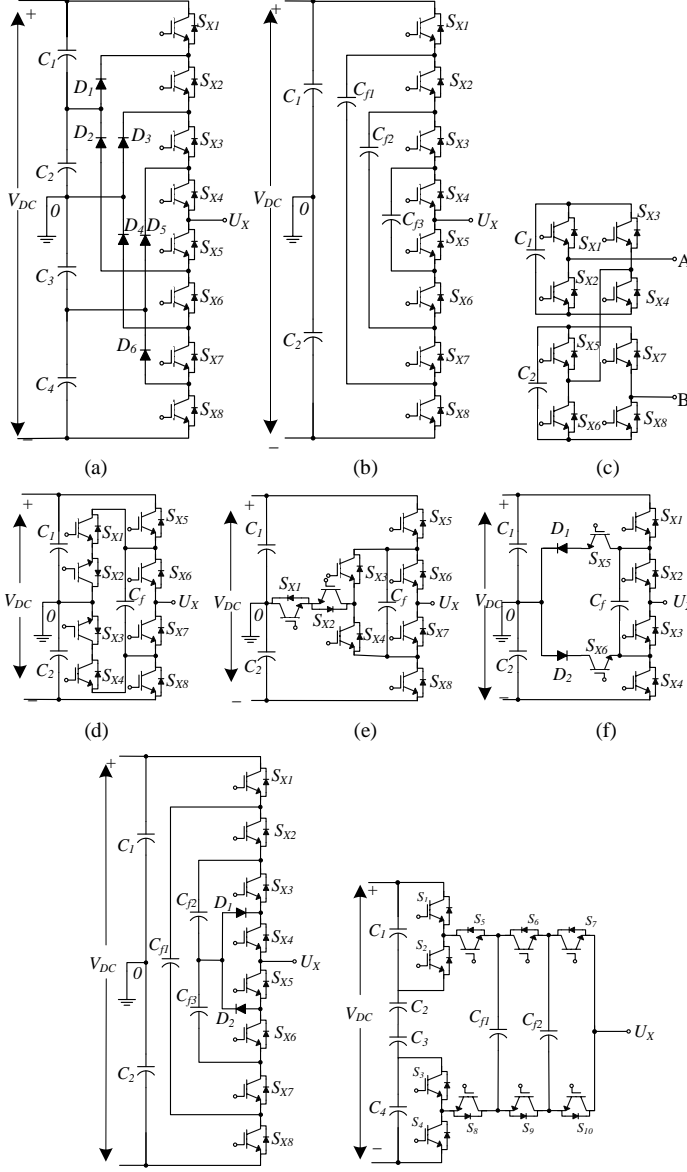


Fig. 1. Phase leg of conventional five-level inverter topologies: (a) 5L-NPC [1]-[5], [9], (b) 5L-FC [5]-[7], (c) Cascaded H-Bridge [3], [8], [11], (d) 5L-ANPC type-II [4], [13], (e) 5L-NPC Type-III [4], [13], (f) 5L-Six Switch ANPC [4], (g) 5L-NNPC [17], and (h) 5L-HC [18]. Here $x \in (R, Y, B)$ phases.

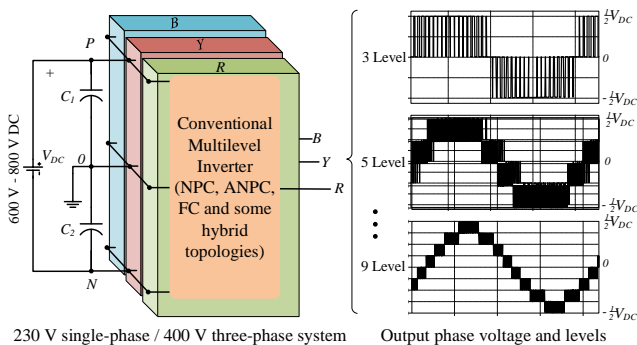


Fig. 2. Conventional multilevel converter showing its typical dc-link voltage requirement and the number of output voltage levels with its peak amplitude.

The paper is organized as follows: Section II presents the concept and analysis of the 5L-ABNPC followed by its operation principle in Section III. A comprehensive comparison with design rules and components selection is presented in Section IV. Simulations and experimental results of the 1.2 kVA single phase prototype are eventually provided in Section V for verification, and the paper is concluded in Section VI.

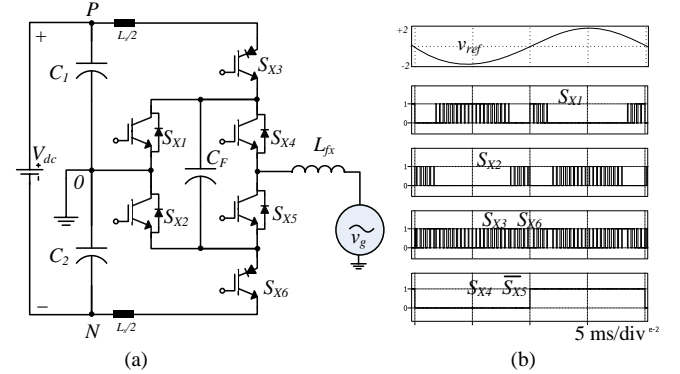


Fig. 3. (a) Configuration of a phase leg of the proposed 5L-ANPC inverter with (b) gate signal for six switches. Here $X \in (R, Y, B)$ phases.

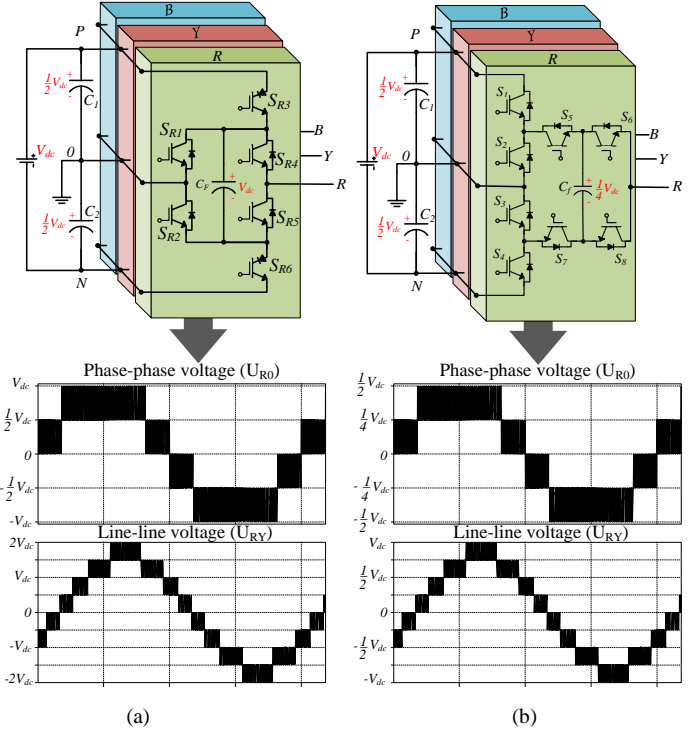


Fig. 4. Illustration of the input dc-link voltage utilization in (a) a proposed 5L-ABNPC inverter, where the dc-bus voltage utilization is $\leq 100\%$, and (b) a conventional 5L-ANPC type-I inverter [7], where the dc-bus voltage utilization is $\leq 50\%$.

II. PROPOSED 5-LEVEL INVERTER

The phase leg of the new *five-level ANPC inverter* consists of six active switches and one capacitor as shown in Fig. 3(a). Similar to the conventional 5L-NPC, 5L-ANPC and 5L-FC topologies, the dc-link consists of two series-connected capacitors C_1 and C_2 , whose voltages are rated at half of the DC voltage ($V_{dc}/2 = 200\text{ V}$ for $V_{dc} = 400\text{ V}$). Among the six switches, the two switches (S_{X3} & S_{X6}) are devices with a bipolar voltage blocking capability, for example, reverse blocking IGBT (RB-IGBT), and the other four (S_{X1} , S_{X2} , S_{X4} & S_{X5}) are standard unipolar voltage devices, such as MOSFET and IGBT, etc. Switches S_{X1} and S_{X4} or S_{X2} and S_{X5} form a bidirectional current carrying paths, which connects the AC terminal with the dc-link mid-point “0” (DC neutral point). The floating capacitor C_F charges through S_{X3} and S_{X6} in every

switching cycle from the input supply V_{dc} to create a virtual dc-bus (Siwakoti-H inverter operating principle) for 2nd level ($0.5V_{dc}$ to V_{dc} or $-0.5V_{dc}$ to $-V_{dc}$) in the output voltage waveform. With this and by appropriately switching dc-link capacitors C_1 and C_2 , five output voltage levels $+V_{dc}/2$, $+V_{dc}$, 0 , $-V_{dc}/2$ and $-V_{dc}$ are achieved, which are defined respectively as +2, +1, 0, -1 and -2. A small quasi-resonant inductor L_s (10 nH - 1 μ H) may be added in the capacitor charging loop, which limit the charging current in the capacitor and can be considered as a wire when the converter enters in the steady state at each voltage level. The corresponding modulating and switching signals are shown in Fig. 3 (b). A schematic of the complete three-phase inverter with its corresponding phase voltage and 3L-line voltage of the inverter is illustrated in Fig. 4(a). Fig. 4(b) shows a traditional counterpart - a conventional 5L-ANPC type-I inverter (implemented in ACS 2000 from ABB) [7], where the dc-bus voltage utilization is $\leq 50\%$. To make further analysis and comparison, V_{dc} is defined as the dc-link voltage of the proposed 5L ANPC, and V_{DC} is the dc-link voltage of the conventional 5L-NPC, 5L-ANPC and 5L-FC topologies, where $V_{dc} = V_{DC}/2$.

Some of the prominent features of the new six-switch five-level ANPC inverter includes:

- i) Reduces the input dc-link voltage (V_{DC}) requirement by two-folds, *i.e.* it requires half of the input voltage compared to traditional NPC, ANPC and Flying Capacitor topologies. This will have huge impact on the system design, cost, efficiency, reliability and power density. It may helps to reduce the high voltage insulation and spacing requirements and it offers better voltage waveforms at the output.
- ii) Reduces the number of components (both active and passive). Only six active switches are used.
- iii) Voltage stress on switches are the same as the conventional NPC, ANPC and Flying Capacitor inverter family, *i.e.* the max voltage stress on the switch is V_{dc} or $0.5V_{DC}$.
- iv) Voltage stress on the dc-link capacitor reduced by 50%, which reduces the size and Equivalent Series Resistance (ESR) of the capacitor. The natural balance of the capacitor voltage is maintained at normal grid condition.
- v) The inverter can provide the reactive power support to the local grid voltage.

III. OPERATING MODES AND MODULATION STRATEGY

A. Unity power factor operation

The operation of the inverter during positive power region consists of six switching states, which generates five-level voltage at the output based on the capacitor voltages. Fig. 5 shows six different switching states (state A to F) and current paths (blue dotted-line shows the active current path, and violet dotted-line represents C_F charging current path). The level of output voltage, corresponding switching states and current through C_F (i_{CF}) are listed in Table I. The output current is defined as i_{ac} , and U_{xo} represents the output voltage. Out of six switches, four switches (S_{X1} - S_{X3} , and S_{X6}) operates at a switching frequency and two switches (S_{X4} & S_{X5}) are commutating at the line frequency. Fig. 6 shows a modulation scheme for the proposed inverter in unity power factor operation with four carriers and one reference signal to generate the appropriate gating signals for one phase of the inverter. The capacitor C_F charges through the dc-link voltage in State A & D and discharge to the load in State C & F. These charging and discharging states are uniformly distributed over the power cycle and can be switched at every switching cycles to maintain the capacitor C_F voltage to a full V_{dc} . For example, switching state ABAB... generates voltage level from 0 to $+0.5V_{dc}$, whilst precharging the capacitor C_F to V_{dc} for generating the next voltage level ($+0.5V_{dc}$ to V_{dc}). Similarly, the charging and discharging states in level 2 (ACAC...) helps to maintain the capacitor voltage to V_{dc} .

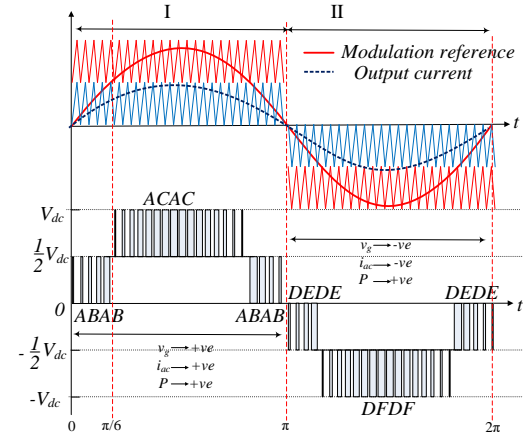


Fig. 6. Level shifted PWM of the 5L-inverter showing phase voltage levels (unity power factor).

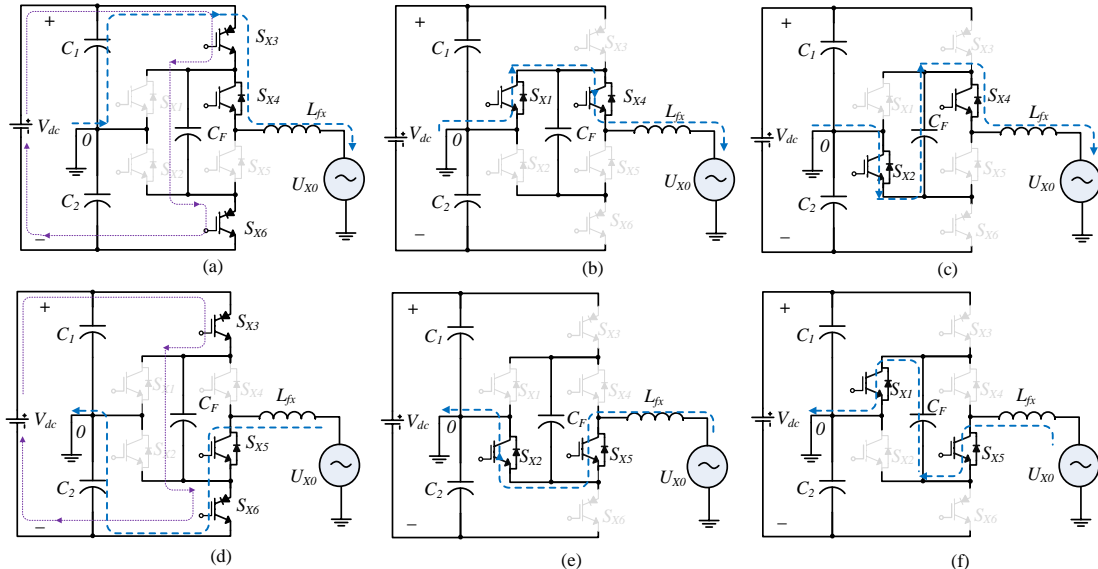


Fig. 5. Six switching states for the proposed inverter: (a) State A: +1, (b) State B: 0, (c) State C: +2, (d) State D: -1, (e) State E: 0, (f) State F: -2 (blue dotted-line represents the active current path and violet dotted-line represents C_F charging current path).

TABLE I
SWITCHING STATES OF THE PROPOSED 5L INVERTER.

Switching States	U_{x0}	S_{X1}	S_{X2}	S_{X3}	S_{X4}	S_{X5}	S_{X6}	i_{CF}
A	$+1/2 V_{dc}$	0	0	1	1	0	1	i_{fc}
B	0	1	0	0	1	0	0	0
C	$+V_{dc}$	0	1	0	1	0	0	i_{ac}
D	$-1/2 V_{dc}$	0	0	1	0	1	1	i_{fc}
E	0	0	1	0	0	1	0	0
F	$-V_{dc}$	1	0	0	0	1	0	i_{ac}

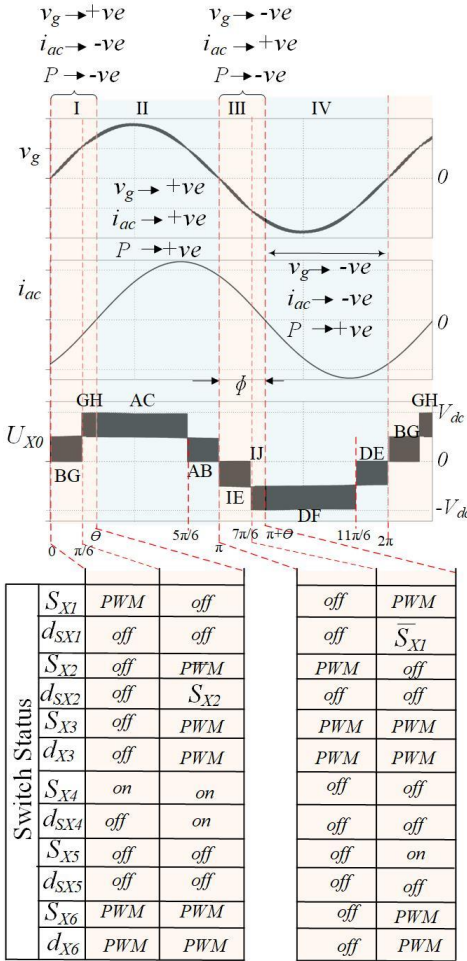


Fig. 7. Non-unity power factor operation of the inverter illustrating its waveforms and switch status.

B. Non-unity power factor operation

The operation of the inverter during the negative power region is shown in Fig. 7, where the polarity of the grid voltage and current (v_g , i_{ac}) are opposite. Regions II and IV belong to the positive power regions (v_g and i_{ac} are in same polarity), while Regions I and III are negative power regions (v_g and i_{ac} are in opposite polarity). The commutation of switches in the negative power region are illustrated in Fig. 8. These are not special or additional switching states on the top of the six switching states as discussed in unity power factor condition, but they are naturally created commutating states by the polarity and direction of the output voltage and current respectively. Red color in the switching device indicates the principal current carrying device, brown color device indicates that the device is off ($v_{gs} = 0$) and blue color indicates the device is naturally turned-off ($v_{gs} = 1$). Here S_{X3} and S_{X6} are unidirectional switches with bipolar voltage capability, but this does not limit the reactive power capability of the inverter. When v_g is positive and i_{ac} is negative, the current free wheels through anti-parallel diode of S_{X4} turning State A (+1 in Fig. 5) to State G (+1 in Fig. 8), where S_{X3} is naturally turned off by the direction of load current. The current free wheels

through anti-parallel diode of S_{X2} and of S_{X4} in State H (+2 in Fig. 8), which used to flows through the main switches (S_{X2} and of S_{X4}) in State C (+2 in Fig. 5). The operation of the inverter in the negative cycle (where i_{ac} is positive and v_g is negative) is similar to the positive cycle. Irrespective of polarity of v_g and i_{ac} , switches S_{X1} with S_{X4} or S_{X2} with S_{X5} form a bidirectional current path during the zero voltage state, which is common in both active and reactive mode of operation. The overall operation of the inverter in both negative and positive power regions is illustrated in Fig. 9. Using Fig. 7, eight operating regions are identified under non-unity power factor condition. The detail operation of the inverter in each region are as discussed below:

- From 0 to $\pi/6$ [$V > 0, i < 0, P < 0$]: Fig. 9(b) illustrate its operation, where switching states BG are used to generate +1.
- From $\pi/6$ to θ [$V > 0, i < 0, P < 0$]: Fig. 9(c) illustrate its operation, where switching states GH are used to generate +2.
- From θ to $5\pi/6$ [$V > 0, i > 0, P > 0$]: Fig. 9(a) illustrate its operation, where switching states AC are used to generate +2.
- From $5\pi/6$ to π [$V > 0, i > 0, P > 0$]: Fig. 9(a) illustrate its operation, where switching states AB are used to generate +1.
- From π to $7\pi/6$ [$V < 0, i > 0, P < 0$]: Fig. 9(b) illustrate its operation, where switching states IE are used to generate -1.
- From $7\pi/6$ to $(\pi + \theta)$ [$V < 0, i > 0, P < 0$]: Fig. 9(c) illustrate its operation, where switching states IJ are used to generate -2.
- From $(\pi + \theta)$ to $11\pi/6$ [$V < 0, i < 0, P > 0$]: Fig. 9(a) illustrate its operation, where switching states DF are used to generate -2.
- From $11\pi/6$ to 2π [$V < 0, i < 0, P > 0$]: Fig. 9(a) illustrate its operation, where switching states DE are used to generate -1.

From the above, all switching states from A to H are being used to generate a complete cycle. Additional redundant switching states A'(+1) and D'(-1) as shown in Fig. 10 can be used to maintain the balance of voltage in C_F during the reactive power mode. Here switching states A and D (where C_{FC} charges) are modified to neutral states A' and F' where C_{FC} neither charges nor discharges whilst producing the required output voltage levels.

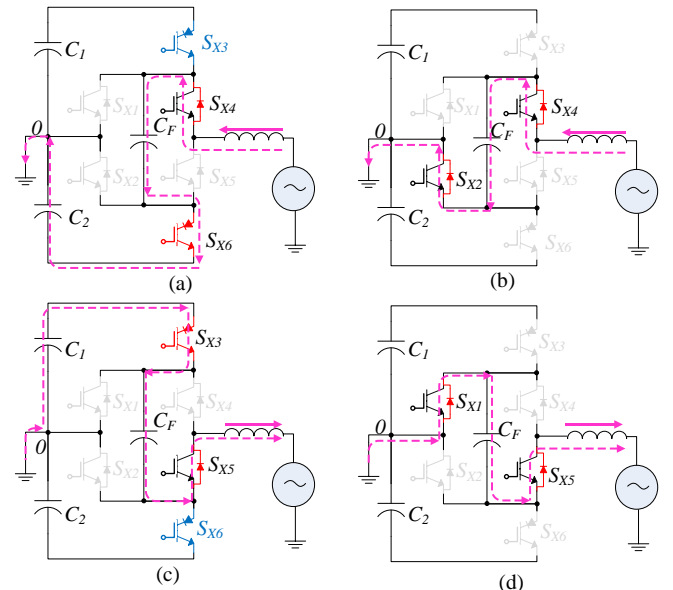


Fig. 8. Commutating states of inverter in non-unity power factor operation (a) State G, and (b) State H, (c) State I, and (d) State J.

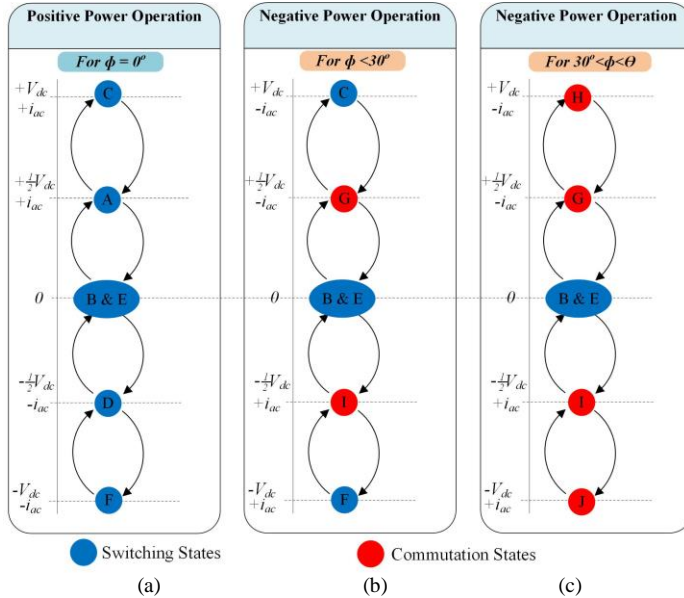


Fig. 9. Overall operation of the inverter illustrating its switching and commutation states at (a) positive and (b) & (c) negative power regions.

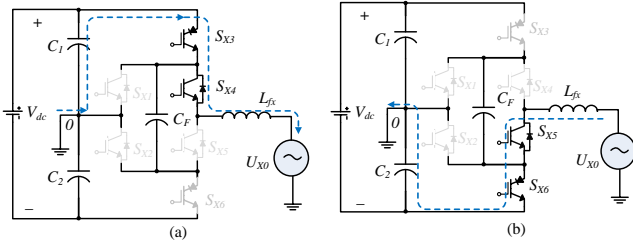


Fig. 10. Redundant switching states A'(+1) and D'(-1) (where no charge/discharge in C_F) by modifying states A(+1) and D(-1) (both charges C_F).

IV. COMPARATIVE SUMMARY AND DESIGN GUIDELINES

A. Comparison with different conventional topologies

A comparative summary of the some of the key features of the proposed 5L inverter with the conventional 5L topologies is presented in Table II. The parameters and numbers of components included are for a phase leg only. The total semiconductor count includes all diodes (antiparallel and/or series), MOSFETs and IGBTs in the topology. For example, the total semiconductor count in the proposed topology is 12, which includes 2 RB-IGBT (2 IGBT + 2 body diodes) + 4 MOSFET (4 MOSFET + 4 anti-parallel diodes). It is evident from the table that the proposed topology requires a minimum number of active and passive components. This effectively reduces the $R_{DS,on}$ and so does the conduction losses in the system. Table III summarizes the equivalent parasitic resistance of the proposed 5L inverter and conventional 5L inverter (Fig. 4(b)). Further compared to the conventional 5L-NPC inverter topologies, the proposed topology reduces the dc-link voltage requirement by two-folds. This will have large impact on the system design, cost, efficiency, reliability and power density.

TABLE III
EQUIVALENT PARASITIC RESISTANCE AT EACH VOLTAGE LEVEL.

Output Voltage	Equivalent parasitic resistance	
	Proposed (Fig. 4(a))	Conventional (Fig. 4(b))
0	$2R_{DS,on}$	$3R_{DS,on}$
± 1	$2R_{DS,on} + R_{DS} + ESR_C$	$3R_{DS,on} + ESR_C + ESR_{CF}$
± 2	$2R_{DS,on} + ESR_{CF}$	$3R_{DS,on} + ESR_C$

Table IV presents a comparative summary of the proposed 5L inverter with the conventional 5L-inverter topologies in terms of

voltage stress and the device switching frequency. Considering scope and brevity, topologies which requires more than eight active switches are excluded from this comparison. It is evident that maximum two active switches are in series during any mode of operation. This reduces the total $R_{DS,on}$ and the corresponding conduction losses.

The comparison of loss and efficiency analysis is not a straight forward due to the difference in the dc-link voltage requirement in the conventional circuit and the proposed circuit. However, to make a fair comparison of loss and efficiency analysis of two different systems, two different cases are considered. In Case-I, the input voltage and power of the both systems are set to 800 V and 1.5 kW respectively, whilst keeping the power factor ($\cos\phi = 1$), switching frequency (20 kHz), modulation index ($M = 0.85$), and device parameters same. Table V summarizes the losses in the switches and diodes of some of the conventional topologies and the proposed topology. The losses are identical in all topologies and hence the efficiency. In Case-II, two similar systems: one with two-stage converter (dc-dc front-end boost converter + conventional buck type multilevel converter as shown in Fig. 11) and the other with a single-stage system (dc-ac system using the proposed topology) is considered. Parameters such as the input voltage ($V_{in} = 400$ V), load (1-2 kVA), power factor ($\cos\phi = 1$), switching frequency (20 kHz), modulation index ($M = 0.85$), and output voltage (v_{ac}) are set identical for both cases. To match the input voltage (400 V) with the dc-link voltage of the conventional multilevel converter (800 V) an additional front-end boost dc-dc converter is required as shown in Fig. 11. In general, these multi-stage power conversion approach reduce the system efficiency and reliability, whilst increasing the size and cost of the system. Therefore, a single-stage dc-ac power converter with the proposed topology with boost capabilities offers an interesting alternative compared to two-stage approach [6]. These two systems are modelled and simulated in PLECS. The proposed 5L-ABNPC improves the overall efficiency of the system by 2-3% over a wide range of load. Here it is important to note that high efficiency is not only rewarding from a power output standpoint, but it also reduces the thermal burden on the inverter. Hence, this further reduces the cooling requirement and the size of the grid connected inverter system.

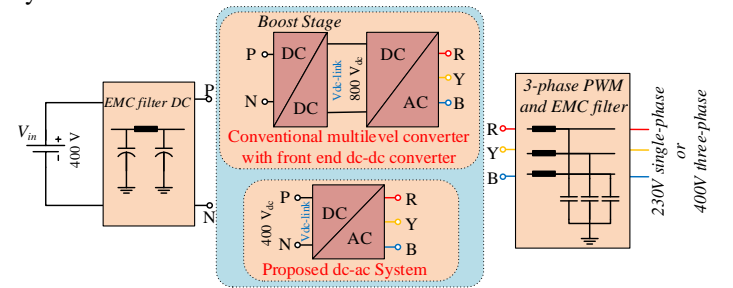


Fig. 11. Illustration of conventional two-stage converter (dc-dc + dc-ac) system and single-stage (dc-ac) system with proposed inverter topology.

B. Design Guidelines and Components Selection

The voltage and current ratings of the active switches and diodes can be deduced from Table VI. However, to retain a comfortable safety margin, voltage and current ratings of the selected power devices should therefore be set at 150% of their theoretically calculated values.

It should also be noted that the switches in the capacitor-charging path (S_{X3} and S_{X6}) are burdened by the capacitor charging current and the load current. The charging current depends on the duty cycle $d(t)$ of the referred switch in the current path, load current $i_{ac}(t)$ and δ , where

TABLE II
COMPARATIVE SUMMARY OF THE PROPOSED 5L-BOOST ANPC WITH THE CONVENTIONAL 5L-INVERTER TOPOLOGIES (ONE PHASE) IN TERMS OF NUMBER OF COMPONENTS AND DC-LINK VOLTAGE REQUIREMENTS.

Parameters	Proposed	Fig. 1(a)	Fig. 1(b)	Fig. 1(c)	Fig. 4(b)	Fig. 1(d)	Fig. 1(e)	Fig. 1(f)
No. of Semiconductors	12	22	16	16	16	16	16	12
No. of Capacitors	3	4	5	2	3	3	3	3
DC- link voltage required for the same output voltage (3-ph out)*	$V_{dc} = \frac{1}{2} V_{DC}$	V_{DC}	V_{DC}	V_{DC}	V_{DC}	V_{DC}	V_{DC}	V_{DC}

*Note: $V_{dc} = 400$ V is the nominal dc-link voltage of the proposed 5L-Boost ANPC, and $V_{DC} = 800$ V is the nominal dc-link voltage of the conventional 5L-NPC, 5L-ANPC and 5L-FC topologies.

TABLE IV
COMPARATIVE SUMMARY OF THE PROPOSED 5L-BOOST ANPC WITH THE CONVENTIONAL 5L-INVERTER TOPOLOGIES IN TERMS OF VOLTAGE STRESS AND THE DEVICE SWITCHING FREQUENCY.

Devices	Type I 5L-ANPC [7]		Type II 5L-ANPC[13]		Type III 5L-ANPC[13]		6S-5L-ANPC [4]		Proposed 5L-Boost ANPC	
	Voltage Stress	Switching Frequency	Voltage Stress	Switching Frequency	Voltage Stress	Switching Frequency	Voltage Stress	Switching Frequency	Voltage Stress	Switching Frequency
S _{X1}	0.5V _{DC}	f_{Line}	0.5V _{DC}	f_{Line}	0.25V _{DC}	f_s for half f_{Line}	0.75V _{DC}	f_s for half f_{Line}	0.5V _{DC}	f_s for half f_{Line}
S _{X2}	0.5V _{DC}	f_{Line}	0.25V _{DC}	f_s for half f_{Line}	0.25V _{DC}	f_s for half f_{Line}	0.25V _{DC}	f_s	0.5V _{DC}	f_s for half f_{Line}
S _{X3}	0.5V _{DC}	f_{Line}	0.5V _{DC}	f_{Line}	0.25V _{DC}	f_{Line}	0.25V _{DC}	f_s	0.25V _{DC}	f_s
S _{X4}	0.5V _{DC}	f_{Line}	0.25V _{DC}	f_s for half f_{Line}	0.25V _{DC}	f_{Line}	0.75V _{DC}	f_s for half f_{Line}	0.5V _{DC}	f_{Line}
S _{X5}	0.25V _{DC}	f_s	0.75V _{DC}	f_s for half f_{Line}	0.75V _{DC}	f_s for half f_{Line}	0.5V _{DC}	f_{Line}	0.5V _{DC}	f_{Line}
S _{X6}	0.25V _{DC}	f_s	0.25V _{DC}	f_{Line}	0.25V _{DC}	f_s	0.5V _{DC}	f_{Line}	0.25V _{DC}	f_s
S _{X7}	0.25V _{DC}	f_s	0.25V _{DC}	f_{Line}	0.25V _{DC}	f_s	-	-	-	-
S _{X8}	0.25V _{DC}	f_s	0.75V _{DC}	f_s for half f_{Line}	0.75V _{DC}	f_s for half f_{Line}	-	-	-	-
D _{X1}	-	-	-	-	-	-	0.25V _{DC}	f_s for half f_{Line}	0.25V _{DC}	f_s
D _{X2}	-	-	-	-	-	-	0.25V _{DC}	f_s for half f_{Line}	0.25V _{DC}	f_s
C ₁	0.5V _{DC}	-	0.5V _{DC}	-	0.5V _{DC}	-	0.5V _{DC}	-	0.25V _{DC}	-
C ₂	0.5V _{DC}	-	0.5V _{DC}	-	0.5V _{DC}	-	0.5V _{DC}	-	0.25V _{DC}	-

TABLE V
COMPARISON OF LOSS IN THE PROPOSED TOPOLOGY WITH SOME OF THE CLOSE CONVENTIONAL TOPOLOGIES (W).

Devices	5L-ANPC Type-I [7]			5L-6 Switch ANPC [4]			Proposed		
	C	S	Total	C	S	Total	C	S	Total
S _{X1}	0.65	0.18	0.83	0.2	0.05	0.25	0.19	0.27	0.46
S _{X2}	0.22	0.035	0.255	0.2	0.05	0.25	0.19	0.287	0.477
S _{X3}	0.22	0.035	0.255	0.6	0.17	0.77	0.32	0.2	0.52
S _{X4}	0.65	0.18	0.83	0.7	0.17	0.87	0.45	0	0.45
S _{X5}	0.86	0.002	0.862	0.7	0.17	0.87	0.45	0	0.45
S _{X6}	0.86	0.17	1.03	0.6	0.17	0.77	0.32	0.2	0.52
S _{X7}	0.86	0.17	1.03	NA	NA	NA	NA	NA	NA
S _{X8}	0.86	0.002	0.862	NA	NA	NA	NA	NA	NA
D _{X1}	NA	NA	NA	1.05	0	1.05	1.5	0	1.5
D _{X2}	NA	NA	NA	1.05	0	1.05	1.5	0	1.5
Total Loss (W)			5.95			5.88			5.877

Note: C = conduction loss, S = switching loss, NA = Not Applicable.

$$d(t) = M \sin(\omega t), \quad (1)$$

$$i_{ac}(t) = I_{ac,max} \sin(\omega t), \quad (2)$$

$$\text{and, } \delta = C_{FC}/C_{DC}. \quad (3)$$

Here, $C_{DC} = C_1 = C_2$ is the dc-link capacitance of the circuit and is calculated considering the permissible voltage ripple across the dc-link (ΔV_{dc}) as

$$C_{DC,min} \geq \frac{I_{dc}}{2f_s \Delta V_{dc,max}}. \quad (4)$$

From (3) and (4), $C_{FC,min}$ can be calculated as

$$C_{FC,min} \geq \frac{\delta V_{dc}}{2f_s R_o \Delta V_{dc,max}}, \quad (5)$$

where, f_s is the switching frequency, R_o is the load resistance and $\Delta V_{dc,max}$ is the allowable voltage ripple into consideration. It is worth noting that the maximum voltage ripple occurs when the load is purely resistive. Once the capacitance is determined under purely resistive conditions, the voltage ripple and hence the required capacitance will be smaller for an inductive load. Fig. 12 shows the curves of minimum capacitance versus the load resistance at different ripple factors. As expected, the size of capacitor increases with the increasing rated output power and hence it keeps the voltage ripple within an allowable range.

The maximum value of the charging current can be calculated as (6), where M is the modulation index and $I_{ac,max}$ is the maximum amplitude of the load current. The charging current not

only depends on the load, but also on M and δ . The current stress reduces with lower M and higher C_{FC} values. However, small M ($M < 0.8$) reduces the dc-link voltage utilization factor and large C_{FC} ($\delta > 4$) increases the cost and size of the capacitor. As a result, a compromise should be made to have a low current stress, while utilizing the dc-link voltage and the associated cost and size of the flying capacitor in the circuit.

$$i_{FC,max} \approx \frac{M}{1-M} \frac{1+\delta}{1+2\delta} I_{ac,max}. \quad (6)$$

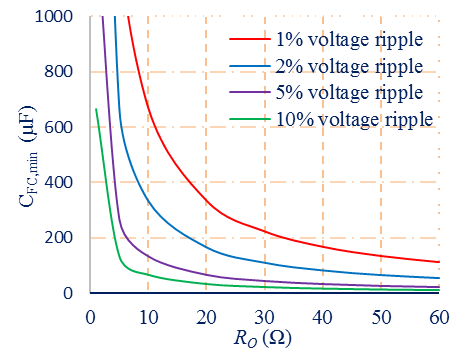


Fig. 12. $C_{FC,min}$ versus R_o at different voltage ripple factor ($V_{dc} = 400$ V, $\delta = 2$, $f_s = 15$ kHz).

Since, the flying capacitor C_{FC} charges in both positive and negative cycle and also in both +1 and +2 levels or -1 and -2

levels. This helps to distribute the charging current throughout the power cycle. However, in order to keep the charging current within the limit, a small inductor L_s in the range of 10 nH - 1 μ H (such as Coilcraft SER2000 Series High Current Shielded Power Inductors) may also be inserted in the circuit as used in [15]. Hence, with appropriately chosen M , δ and L_s ($0.8 \leq M \leq 0.95$, $1 \leq \delta \leq 4$, and $10 \text{ nH} \leq L_s \leq 1 \mu\text{H}$), the current on the relevant switches in the charging current path is approximately estimated to be between $2.5I_{ac,max}$ to $4I_{ac,max}$. This is generally the case of any boost type converters.

In practical applications for any converter/inverter, switching devices exist certain turn-on and turn-off time delay. To prevent a short circuit in the dc-link capacitors and the flying capacitor (C_F) due to this time delay, a switching delay time is required to insert into PWM signals. This dead time introduces a voltage error at the phase terminal of inverter, which is dependent on the polarity of the phase current. The voltage error increases harmonic components of output voltage and decreases control performance. Therefore, similar to any conventional converter, a dead-time compensation is recommended to prevent voltage error [19].

TABLE VI
SUMMARY OF VOLTAGE AND CURRENT STRESS OF THE PROPOSED TOPOLOGY.

Switches	Voltage Stress	Current Stress
S_{X1}	$+V_{dc}$	$\approx I_{ac,max}$
S_{X2}	$+V_{dc}$	$\approx I_{ac,max}$
S_{X3}	$\pm 0.5 V_{dc}$	$\approx \left[\frac{M}{1-M} \frac{1+\delta}{1+2\delta} + 1 \right] I_{ac,max}$
S_{X4}	$+V_{dc}$	$\approx I_{ac,max}$
S_{X5}	$+V_{dc}$	$\approx I_{ac,max}$
S_{X6}	$\pm 0.5 V_{dc}$	$\approx \left[\frac{M}{1-M} \frac{1+\delta}{1+2\delta} + 1 \right] I_{ac,max}$

V. SIMULATION AND EXPERIMENTAL RESULTS

To verify the concept of the proposed inverter circuit and the theoretical analysis, PLECS simulations have been carried out. The parameters and component values used for both simulations and the experimental prototype are listed in Table VII. Fig. 13 shows the steady state output voltage, load current, voltage across FC and dc-link capacitors, as well as the voltage and current stress of the switches. The fourth trace in Fig. 13(a) shows an unfiltered 5-level voltage, which is filtered out to get a pure sinusoidal voltage and current at the load. The inverter produce RMS voltage of about 230 V for 400 V dc-link voltage. Under unity power factor, the current and voltage are in phase. The output current has a sinusoidal without distortion (THD < 2 %). Under the normal operating conditions (230 V, 50 Hz), the voltage across the dc-link capacitors is naturally balanced around its reference value $V_{dc}/2 = 400/2 = 200 \text{ V}$ (Fig. 13(a)). However, a dedicated controller is required to improve the transient performance and to balance the capacitor voltage under extreme operating conditions, such as under low fundamental frequency operations. Further as shown in Fig. 13(c) & (d), the voltage and current stress are in agreement with the analysis made in the earlier sections.

The capacity of delivering reactive power has also been successfully tested for both lagging and leading power factors. Fig. 13 (b) shows the operation of the inverter in lagging power factor $\phi_{pf} = -45^\circ$. Hence, without considering any special consideration (additional switching devices or switching sequence) or modulation technique, the inverter is capable of generating 5-level output voltage; which when filtered out to get

pure sinusoidal voltage and current. This verify the seamless operation of the inverter as illustrated in Fig. 9 for any power factor angle.

TABLE VII: PARAMETERS USED FOR SIMULATION AND MEASUREMENT.

Description	Value/Parameter Used
Input Voltage (V_{dc})	380 V
Output voltage (v_{ac})	230 V
Power Rating (P_o)	1.2 kVA
Carrier frequency (f_s)	20 kHz
Line frequency (f)	50 Hz
dc-link capacitor (C_1 & C_2)	470 μ F, 250 V
Flying capacitor (C_{FC})	470 μ F, 450 V
Filter inductor (L_f) & capacitor (C_f)	0.32 mH and 2.2 μ F
Switches ($S_{X1} - S_{X6}$)	SCT3022AL
Diode (D_{X1} & D_{X2})	C5D50065D
Load (resistor and inductor)	1.2 kVA (30-60 Ω , 35 mH)

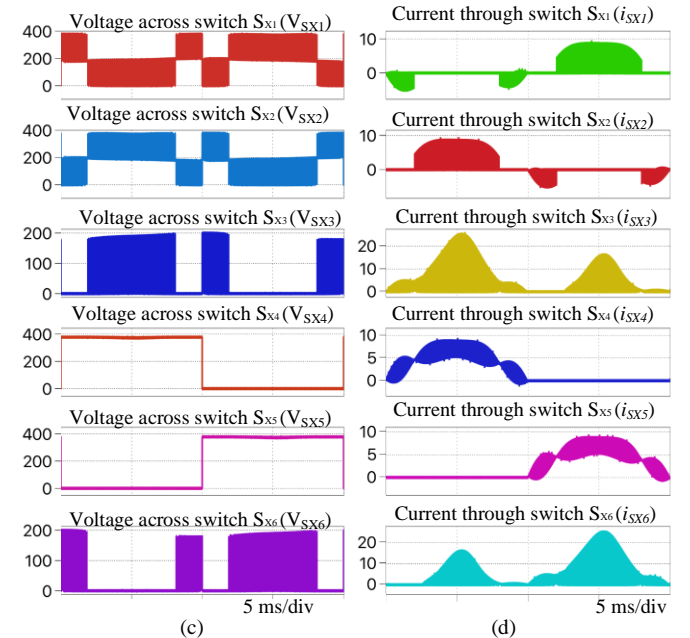
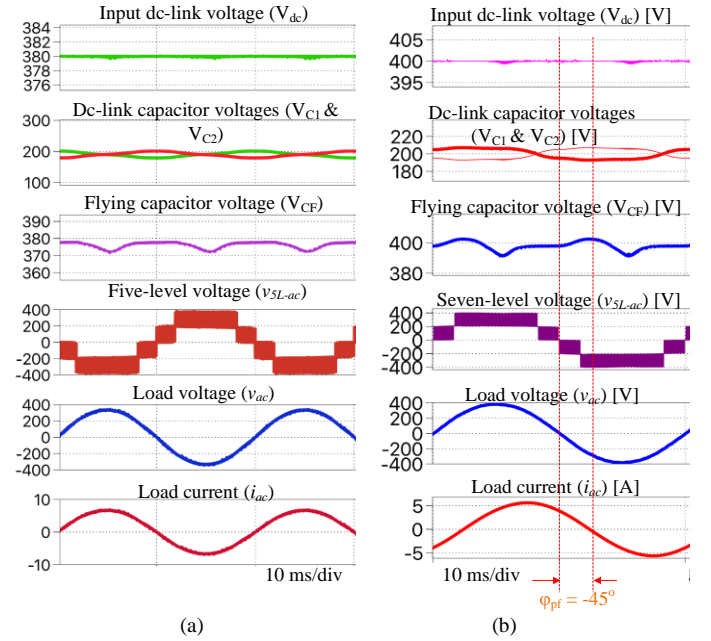


Fig. 13. Key simulated waveforms of the proposed five-level converter showing (a) input/output voltage/current at unity power factor and (b) input/output voltage/current at lagging power factor of $\phi_{pf} = -45^\circ$, (c) voltage across switches and (d) current through the switches.

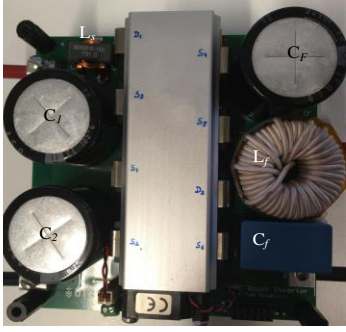


Fig. 14. Picture showing the prototype of a 1.2 kVA (single-phase) inverter.

As a follow-up, based on the satisfactory simulation results and to verify and validate the practicality of the proposed 5L inverter, a scaled-down and very compact 1.2 kVA prototype was developed as shown in Fig. 14. All switches are 650 V SiC devices (SCT3022AL) from ROHM Semiconductor. Fig. 16 show the experimental results under unity power factor condition.

It can be seen that the inverter is capable of generating a five-level output voltage with a clean sinusoidal voltage and current.

Fig. 15 (a) & (b) shows the inverter input/output voltage and current waveforms with clear 5 levels in the output voltage. Channel 2 of the oscilloscope shows the input current of the inverter, which is continuous with a peak amplitude of around 5 A. Note that, a dc-link voltage of 380 V magnitude is applied to achieve maximum ac voltage of 230 VRMS. Hence, unlike the conventional 5L topologies with nominal dc-link of 800 V, the voltage boosting capability is a major achievement of the proposed topology. The measured output current THD is 1.8%.

As shown in Fig. 15 (c) & (d), the voltage stress on device corroborates with the earlier analysis and simulated results. Fig. 15 (e) also shows the voltages of two dc-link capacitors and flying capacitor capacitor voltage. The measured peak-to-peak FC voltage ripple is 8 V ($= 10 \text{ V}/400 \text{ V} = 2.5\%$) and dc-link capacitor line-frequency voltage ripple is 20 V ($= 20 \text{ V}/200 \text{ V} = 10\%$). The balanced FC and dc-link capacitor voltages verify the modulation method and confirm the advantage of the self-balancing in the proposed circuit. In addition, as shown in Fig. 15

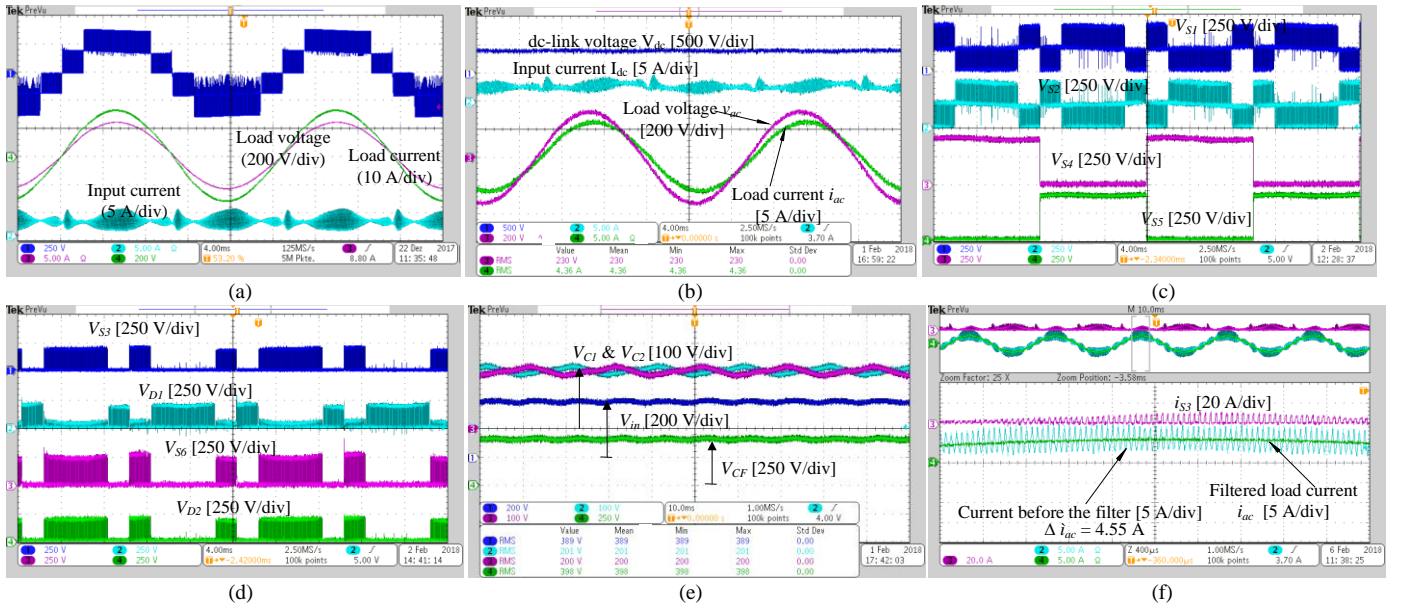


Fig. 15. Measured waveforms under unity power factor condition showing (a) & (b) inverter input/output voltage/current waveforms and dc-link voltage, (c) & (d) voltage stress on the semiconductor devices, (e) dc-link voltage, flying capacitor voltage, and upper and lower DC-link capacitor voltages, and (f) output currents (before and after the filter).

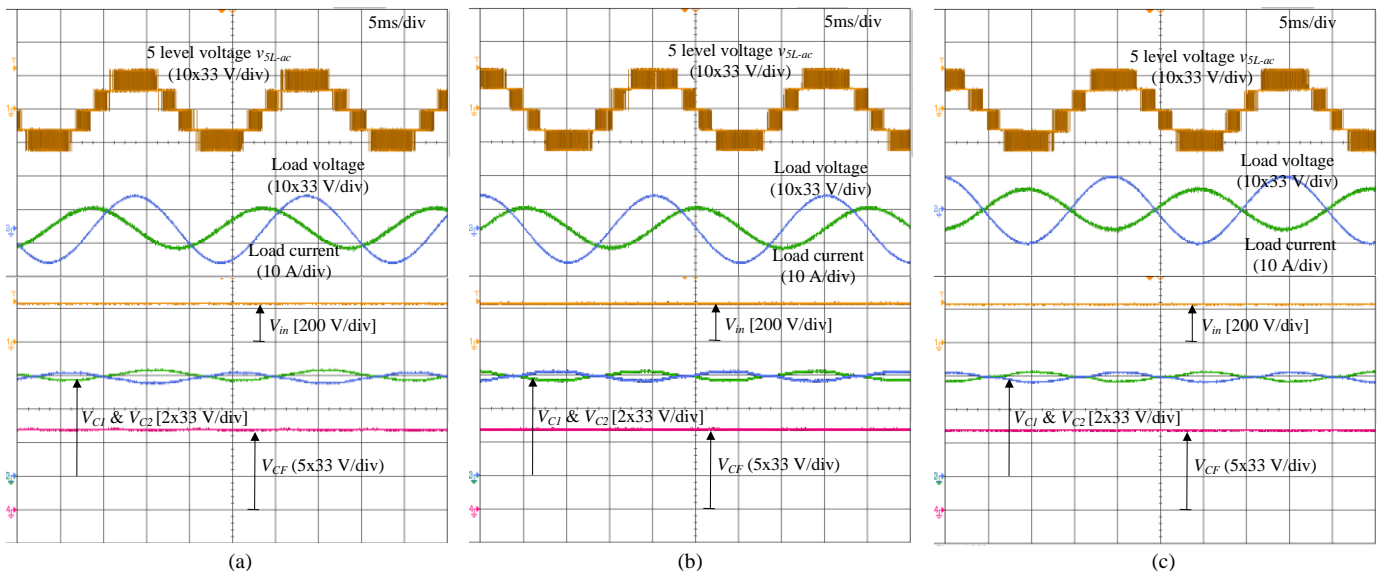


Fig. 16. Measured waveforms under reactive power condition showing inverter input/output voltage and current waveforms with dc-link voltage, flying capacitor voltage, and upper and lower dc-link capacitor voltages at (a) $\phi = -90^\circ$, (b) $\phi = +90^\circ$ and (c) $\phi = 180^\circ$.

(f), a small LC filter provide a better ripple attenuation with a maximum peak-to-peak amplitude of 4.55 A.

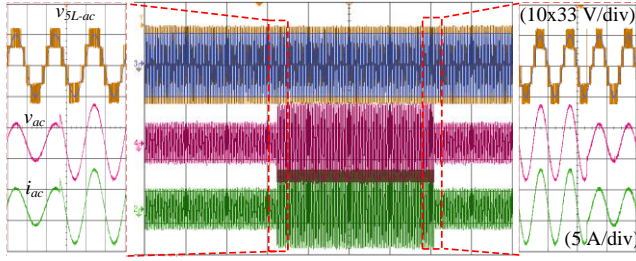


Fig. 17. Transient response of the converter with the load change (from half to full load).

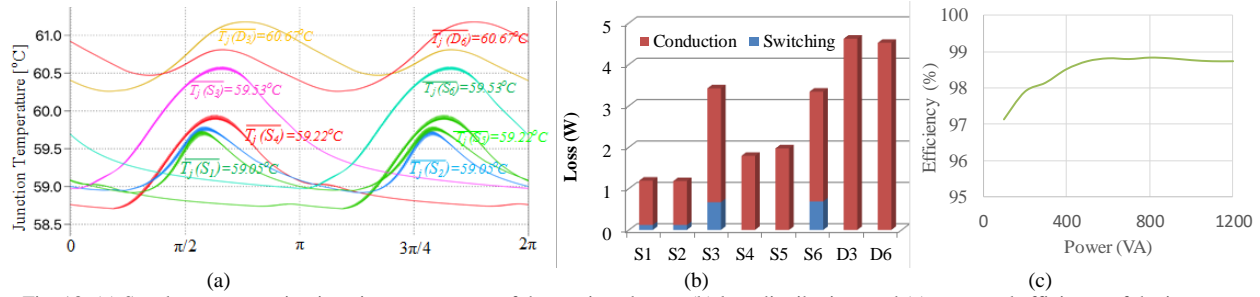


Fig. 18. (a) Steady state operating junction temperature of the semiconductor, (b) loss distribution, and (c) measured efficiency of the inverter.

Similar to any flying capacitor type multilevel converter, the balancing of the capacitor voltage is increasingly difficult at higher power factor angle ($\varphi > \pm 90^\circ$). Hence, without proper voltage balance control [22], the natural balanced of the flying capacitor in the proposed six-switch 5-level inverter is limited by the power factor angle $\varphi < \pm 90^\circ$. Nonetheless, the proposed converter can be operated in any power factor using method discussed in [22] or replacing S_{x3} and S_{x6} with bidirectional switches. The operation of the proposed inverter in non-unity power factor is demonstrated in Fig. 16. The ripple in the capacitor voltage is same as in the unity power factor condition. A transient operation of the inverter during the load change is also demonstrated in Fig. 17. The inverter produces good quality voltage and current waveform without distortion ($\text{THD} < 1.8\%$). Finally, the averaged power loss distribution and the operating junction temperature (T_j) of the individual switching elements in a phase-leg are shown in Fig. 18(a). A PLECS software was used for thermal analysis considering a constant ambient temperature, T_A , of 40°C with uniform temperature distribution across the heat sink. As expected, the switches in the capacitor-charging path have higher loss (conduction) and hence relatively higher temperature ($\Delta T_j \approx 2^\circ\text{C}$) than the other switches. Fig. 18 (b) show similar findings and the loss distribution across the switching components. Fig. 18(c) shows the measured efficiency of the inverter at different output power levels. The efficiency of the inverter is $97.8\% \pm 1\%$ for a wide range of load.

VI. CONCLUSIONS

In this paper, a novel six-switch five-level ANPC inverter is proposed. The modulation techniques and operation under both active and reactive power factor conditions are systematically analyzed and presented. Comparative analysis and design guidelines are presented in depth followed by simulation and experimental verification.

Compared to conventional multilevel inverter topologies, the novel inverter topology reduces the required active power devices down to six per phase and reduces the dc-link voltage requirement by 50%. Further, this reduces the voltage stress on

the dc-link capacitor, which reduces the cost and size of the system design. In addition, the inverter can compensate the reactive power required by the grid. However, the proposed topology draws higher RMS current, which increase the conduction losses in the system specially on the diodes.

Computer simulations and experimental results validates the expected performance of the system for higher power application. Compared to the existing 5L inverter topologies, the performance demonstrated by the new inverter is presently incomparable, which makes it an appropriate topology for a wide-range of power conversion applications, for example, variable-speed drive system, electric vehicles (V2G/G2V technologies), grid-connected renewable energy systems.

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